COVER STORY:
Gigabit Ethernet:
EMC-Compliant Implementation

PAGE 6

ALSO IN THIS ISSUE

Li-Fi Lights Up the Wireless Industry
PAGE 18

Hardware Pioneers
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PAGE 41

Exclusive Interview:
STMicroelectronics’ Remi El-Ouazzane
PAGE 54
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EDITOR'S LETTER

EU Turns Rivals into Allies

Germany is a favorite. After Intel got the go-ahead this summer to expand its planned footprint in Magdeburg, TSMC received the green light for a joint-venture fab in Dresden. The pledges come at a make-or-break moment for the EU’s long-term competitiveness.

A sense of responsibility and a sentiment of “never again” emerged as Europe faced severe semiconductor supply chain disruptions and challenges in the post-Covid-19 economy. Over the years, Europe had ceded vast amounts of its market share in semiconductor manufacturing, and its reliance on imports had become particularly troublesome in industries such as automotive and consumer electronics. The EU Chips Act, proposed in February 2022 and passed into law in July 2023, aims to enhance resilience, strategic autonomy and security of supply in semiconductors.

In the semiconductor industry, working in unison and rallying collective strengths have often paid off. In this respect, the creation of a European chip champion has been a recurring theme. In 2008, Joseph Borel, former executive vice president of central R&D at STMicroelectronics, proposed that Europe’s top three chip companies, NXP, ST and Infineon, consolidate into one European super chip company. In a 12-page proposal titled "Nanotechnologies in Europe: There is room for a single profitable shared application-driven foundry," Borel urged the competitors to stop operating individually and join forces to achieve critical mass on a scale close to that of then semiconductor market leader Intel and larger than that of second-ranked Samsung.

In May 2013, the EC committed €5 billion of public money as part of the Electronic Components and Systems for European Leadership Joint Technology Initiative. Ten years later, however, the "Airbus of chips" is a distant memory, and joint ventures are being set up with global players. Instead of just going head-to-head, TSMC, Bosch, NXP and Infineon have decided to join forces under a joint venture (JV) agreement. The announcement came just days after semiconductor companies Bosch, Infineon, Nordic Semiconductor, NXP and Qualcomm agreed to form a JV aimed at accelerating the adoption of RISC-V and hardware development—once more, in Germany.

But how to partner with longtime rivals for a win-win? According to the European University Institute’s Public Procurement Regulation, a JV is an entity formed between two or more parties to undertake economic activity together. Both parties agree to create a new entity by contributing equity. They then share in the revenues, expenses and control of the enterprise.

When companies decide to set up a JV, a crucial first step is to determine the appropriate level of ownership and control. The TSMC board of directors’ meeting resolutions outline an “Approved equity investment of no more than €3,499.93 million to a TSMC-majority-owned subsidiary, European Semiconductor Manufacturing Company (ESMC) GmbH, in Germany to provide foundry services.” Subsequently, ESMC will be 70% owned by TSMC, with the other companies holding 10% each.

It is too early to say, but what about the revenue- and profit-sharing agreement? What about the production capacity allocation? Does a 10% equity stake entitle the investor to a 10% production capacity allocation?

The construction of the fab is set to begin in the second half of 2024, with production commencing by the end of 2027. A monthly manufacturing capacity of 40,000 300-mm wafers is planned based on TSMC’s 28/22-nm planar CMOS and 16/12-nm FinFET process technologies.

For the sake of domestic security and global competitiveness, the EU turns a blind eye to business rivalries. And as Yole Group CEO Jean-Christophe Eloy appropriately puts it, “Money is on the table. TSMC takes it.”

—Anne-Françoise Pelé, editor-in-chief of EE Times Europe

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Gigabit Ethernet: EMC-Compliant Implementation

Whether in the office or in the factory, Gigabit Ethernet is the networking standard of choice. Two Gigabit Ethernet reference designs from Würth Elektronik provide examples of how the challenges can be met from an RF and EMC perspective.
PARTNER CONTENT

38 Using In-Cabin Radar Solutions for Child Presence Detection

EMBEDDED

41 And That’s a Wrap: Hardware Pioneers Max 2023

44 Startups Help RISC-V Reshape Computer Architecture

47 Three Tools to Speed Your Embedded Development

50 Opinion: How Quantum Computing Can Help Make AI Greener

51 CEO Interview: Intrinsic ID’s Pim Tuyls on Embedded Security

54 Remi El-Ouazzane: ‘A Tsunami of TinyML Devices Is Coming’

PARTNER CONTENT

56 World’s First Professional Cleanroom Biomass Gloves

THE INDUSTRY

58 Opinion: Assessing the U.K. National Semiconductor Strategy

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Gigabit Ethernet: EMC-Compliant Implementation

BY DR. HEINZ ZENKNER, Technical Marketing EMC Consultant, Würth Elektronik eiSos

Whether in the office or in the factory, Gigabit Ethernet is the networking standard of choice. Two new Gigabit Ethernet reference designs from Würth Elektronik provide examples of how the challenges can be met from an RF and EMC perspective.

Over the past few decades, Ethernet has become the global networking standard par excellence, from homes to offices and production floors to cars. Currently, Gigabit Ethernet is the state of the art, so developers of networkable electronic devices cannot avoid implementing a 1-Gbit/s Ethernet interface. Circuit designers can now obtain an optimized circuit design and layout, including all technical data, with the two versions of a Gigabit Ethernet reference design from Würth Elektronik. This facilitates the implementation of a reliable Gigabit Ethernet interface in their target application.

The RD016 reference design includes two interfaces: a USB Type-C (USB 3.1) and a 1-Gbit/s RJ45/Ethernet interface. The Gigabit Ethernet USB adapter has been developed based on the evaluation board EVB-LAN7800LC from Microchip. The circuit is built on a four-layer printed-circuit board and in the present design is powered via the USB interface. The first part of this article presents the technical basics that are necessary for the understanding of the reference designs. The second part describes in detail the 1-Gbit/s Ethernet interface up to the physical (PHY) layer. EMC technical aspects are covered in detail in Application Note ANP116.7

ETHERNET BASICS

Ethernet was first distributed worldwide at 10 Mbits/s over coaxial cable and later over unshielded twisted-pair (UTP) cables at 10BASE-T. Currently, 100BASE-TX (Fast Ethernet, 100 Mbits/s), Gigabit Ethernet (1 Gbit/s), 10 Gigabit Ethernet (10 Gbits/s) and 100 Gigabit Ethernet (100 Gbits/s) are available. For most purposes, Gigabit Ethernet works well with regular Ethernet cables, specifically the CAT 5e, CAT 6 and CAT 6a cabling standards. Those cable types follow the 1000BASE-T cabling standard, also called IEEE 802.3ab.

Because of such factors as network protocol overhead, retransmissions due to collisions on the transmission path and sporadic data errors, the maximum usable data rate under normal conditions is 900 Mbits/s. The average connection speed varies with the hardware structure of the PC, the number of clients at the router and, last but not least, the “quality” of the Ethernet cabling.

Figure 1: Schematic circuit of a 1-Gbit/s Ethernet interface. Only one of four channels is shown in the picture.
**Gigabit Ethernet: EMC-Compliant Implementation**

**BY DR. HEINZ ZENKNER**, Technical Marketing EMC Consultant, Würth Elektronik eiSos

The Gigabit Ethernet USB adapter board is available in two versions. Version V1.0 includes discrete components in the Ethernet interface area. That is, the matching network and the inductor block, consisting of common-mode chokes and transformers, are individual components placed on the PCB (Figure 2).

In the V2.0 version, the aforementioned components are integrated into the housing of the RJ45 socket (Figure 3).

**Gigabit Ethernet Adapter Board**

The Gigabit Ethernet USB adapter board is available in two versions.

- Version V1.0 includes discrete components in the Ethernet interface area. That is, the matching network and the inductor block, consisting of common-mode chokes and transformers, are individual components placed on the PCB.
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**Block Diagram**

The USB 3.1 Gigabit Ethernet controller LAN7800 connects the USB interface with the Ethernet interface as a "bridge" (Figure 4). Thus, only the signaling adaptations and decouplings must be implemented for the wiring of the interfaces. On the USB side, a DC/DC converter is used to generate the 3.3-V supply voltage required for the LAN7800. The LAN7800 needs an additional 4-kbit E²PROM to store the firmware.

**Circuit Elements**

The controller, power supply, and USB 3.1 interface are only touched upon here, as the focus of this article is on the 1-Gbit/s Ethernet interface.

- **Controller**: The LAN7800 is a high-performance USB 3.1- to 1-Gbit/s Ethernet controller with integrated Ethernet PHY. An external 4-kbit E²PROM was added for on-board software.
- **Power Supply (5 V to 3.3 V)**: The controller needs a supply voltage of 3.3 V. This is generated here with the

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**Interface Structure and Required Hardware**

RJ45 interfaces are designed for full-duplex transmission, i.e., simultaneous transmission of send and receive data. This is possible because the connector comprises four pairs of wires, whereby one pair is always required for one direction (differential voltage principle). In principle, impedance is 100 Ω for UTP and 150 Ω for shielded twisted pair (STP) (100BASE-T: IEEE 802.3, e.g., section 39). In the case of branded cables, Categories 5e, 6 and 6a are available both shielded and unshielded, and Categories 7 and 7a are always shielded. For each RJ45 connection, the IEEE standard requires galvanic isolation via a transformer. This transformer protects the devices from damage caused by high voltage on the line and prevents voltage offsets that can result from potential differences between the devices. Figure 1 shows the principal circuit of the interface.

Incoming from the RJ45 interface, the Ethernet signal reaches the transformers via a common-mode choke. Figure 1 shows only one of four channels. The transformer has a center tap, which represents a zero potential from a signal engineering point of view. Unbalances act as voltage at the center tap and are terminated to ground via the 75-Ω resistors, which are DC-decoupled via the capacitor. The transformer has a transformation ratio of 1:1. On the secondary side, the Ethernet signal reaches the PHY via the four channels. Here, too, the impedance is 100 Ω differential, or 50 Ω each to ground (GND). The center tap of the transformer is AC-terminated to ground on the secondary side via capacitors.

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**Figure 2**: Gigabit Ethernet USB adapter board in the discrete version V1.0. The module with the transformers and common-mode chokes is placed next to the RJ45 jack.

**Figure 3**: Gigabit Ethernet USB adapter board in the discrete version V2.0. The module with the transformers and common-mode chokes is integrated in the RJ45 socket.
Gigabit Ethernet: EMC-Compliant Implementation

Figure 4: Block diagram of the Gigabit Ethernet-USB adapter board used in both versions

Figure 5: WE-LAN AQ transformer for galvanic isolation between the PHY and Ethernet network

**requirements, isolation voltages of up to 6 kV can be achieved.**

As there is no functional difference between the two versions, the circuitry of the Gigabit Ethernet interface is explained below using the V1.0 version with discrete components.

**Gigabit Ethernet front end**

LAN transformer X3 in Figure 5 provides DC isolation between the electronics and the network cable. The test voltage for the transformer between the primary and secondary sides is 1,500 Vrms.

The center tap of the primary-side winding, i.e., to the Ethernet port, has the Bob Smith termination mentioned above. For each pair of wires, a 75-Ω resistor is connected to form a "star point"; the entire circuit is then galvanically isolated, connected to the housing ground by means of two 100-pF capacitors connected in parallel. In the literature, one often finds capacitors with a capacity of up to 2 nF, which is a relatively high value in relation to the frequency range. The capacitors should have a dielectric strength of at least 2 kV.

The Bob Smith termination is used to reduce interference caused by common-mode current flows and to reduce susceptibility to interference from unused wire pairs on the RJ45 connector.

The Bob Smith termination is referenced to an impedance of about 145 Ω per wire pair. Given the market availability of many different cable types, the differences in the base impedances of the various cable types and the fact that the cables do not have a constant impedance over their length due to twisting, common-mode chokes were also implemented (Figure 5).

Thus, one transformer and one common-mode choke per channel are connected in module X3. Although these chokes cannot correct the deviations of the impedance matching, they significantly improve the EMC behavior. The circuitry of the elements with passive components and TVS diodes as well as the PCB layout are described in detail.†

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hotonics—the science of creating, manipulating, transmitting and detecting light—is powering some of today’s most important technological advances, with applications ranging from optical communications to imaging, lighting and displays, industrial sensing and automation, life sciences, healthcare, security and safety.

Silicon photonics integration enables cost-effective, low-power optical interconnects in high-performance computing systems and data centers. An ecosystem is forming around light-based interconnects, with established players and new entrants emerging to advance the technology.

Europe has a long history of contributing to the development of photonics technology. This was demonstrated in 2022, when European scientists Alain Aspect and Anton Zeilinger, along with John F. Clauser of the U.S., won the Nobel Prize in Physics "for experiments with entangled photons, establishing the violation of Bell inequalities and pioneering quantum information science."

Europe is now the world’s second largest supplier of photonics components and systems after China, with a 16% share of the global photonics market in 2022, according to an April 2023 report compiled by the European Technology Platform Photonics21.

The global market last year was worth more than US$800 billion—about US$105 billion in photonics components and over US$700 billion in photonics systems, the report found.

In recent years, the European Commission has taken full measure of the potential of photonics technologies to strengthen EU strategic supply chains and reduce trade dependency. Photonics is one the six Key Enabling Technologies selected by the EC and one of 11 co-programmed European Partnerships implemented through the Horizon Europe Strategic Plan. The value of integrated photonic solutions is also recognized by the EU Chips Act, which will accelerate investment in semiconductor chips, including photonic integrated circuits.

The European photonics industry now comprises over 5,000 SMEs and large companies and directly employs more than 400,000 qualified professionals within the EU. These figures are bound to grow, as the current trends are exponential.

In this Special Report, we navigate the European and global innovation ecosystem and shed light on the promise and pitfalls of transmitting data via photons. It includes contributions by Lightelligence and IDTechEx and reflects our discussions with the University of Amsterdam, the U.K. National Physical Laboratory, PsiQuantum, Quantum Computing, pureLiFi, X-FAB, CEA-Leti, Aryballe, TriEye and Coherent.
Moving Time: Bringing Quantum Clocks Out of the Lab

By Rebecca Pool

Portable optical clocks will change the ways in which the world measures time, space and much more.

When quantum clock pioneer Jun Ye created strontium optical lattice clocks so precise that they could measure gravitational redshift on the millimeter scale, time must have stood still, at least figuratively, for physicists everywhere. For starters, the U.S.-based JILA Research Institute professor had tested Einstein’s theory of general relativity, which predicts clocks in a deep gravitational field will tick more slowly than those in a shallower field, to such remarkable precision that he had broken all atomic clock records. And he had achieved the feat within the confines of his lab, in stark contrast to experiments that have taken place using atomic-clock-equipped satellites thousands of miles apart in space.

But while the race to scrutinize fundamental physics with ever more precise quantum clocks proceeds apace, a different mission has emerged: getting these systems out of the lab and into real life, where they can measure more earthly endeavors and phenomena. Think telecommunications, navigation, land movements and more.

Experimental quantum physicist and University of Amsterdam professor Florian Schreck is at the forefront of such development as the head of the recently launched, EU-funded, €7.5 million AQuRA (Advanced Quantum Clock for Real-World Applications) project. Over the next three years, Schreck, fellow researchers and a host of photonics industry players will build and then field-test a wardrobe-sized strontium optical lattice clock.

As Schreck put it, “Atoms are the best time-keeping devices we have … and time measurements using light emitted by atoms can be made extremely precise. Yet the funny thing is, to control [tiny] atoms, we currently need to build the biggest machines in a university lab. Hopefully, in a few years from now, this contrast will be a lot smaller, and you’ll encounter extremely precise, portable quantum clocks in the real world.”

WHAT’S IN A CLOCK?
Atomic clocks measure time using the resonant frequencies of atoms, which act as the “ticks” of the clock. Many atomic clocks, including the world-standard cesium clock at the U.S. National Institute of Standards and Technology (NIST), use clusters of cesium atoms cooled to temperatures approaching absolute zero. Shine laser light on these atoms and they emit light that oscillates 9.2 billion times every second. Other atomic clocks harness elements like strontium and ytterbium, which emit light at higher frequencies and therefore tick even more precisely.

Strontium optical lattice clocks, pioneered by Ye and Hidetoshi Katori, a professor and physicist at the University of Tokyo, emerged some two decades ago. These atomic clocks are also called quantum clocks, as they measure quantum fluctuations, or narrow energy transitions, within the actual strontium atoms. In these clocks, thousands of ultracold strontium atoms are trapped in a lattice of intense laser light, inside an ultra-high-
AQuRA, we’re really aiming to take the performance of transportable clock technology to a similar level as existing clocks that occupy an entire laboratory,” Schreck said. “A transportable clock such as this will become really interesting.”

COMMERCIAL FOCUS
Schreck is no stranger to atomic clocks, having led the pan-European consortium iqClock (short for “integrated quantum clock”), which developed a transportable strontium optical lattice clock and helped to kickstart portable atomic clock development across the continent. With AQuRA, Schreck and colleagues intend to build a more precise, transportable clock. And critically, they have their sights firmly set on commercialization, intending to provide Europe with a market edge in compact atomic clocks.

To this end, most of their clock’s key components will come from industry. For example, the all-important lasers—used to cool, trap and excite the device’s time-keeping strontium atoms—are being supplied by key European optics players, including Denmark’s NKT Photonics, France’s iXblue, the Netherlands’ QuiX Quantum, Finland’s Vexlum and Germany’s Menlo Systems. Menlo Systems, known for commercializing the Nobel Prize–winning optical frequency combs used to control timing in optical clocks, will also lead AQuRA’s systems integration.

The partners plan to build a strong European supply chain that will underpin optical atomic clocks and other quantum technologies, including sensing, computing and simulation platforms. “I would hope that if there is a customer out there who would like to purchase our atomic clock, our industry partners could provide this with very little effort,” Schreck said.

Tokyo University’s Katori, who is also affiliated with the Quantum Metrology Laboratory at Japan’s Riken Institute, has already developed robust, transportable strontium optical lattice clocks with \(10^{-18}\) precision. Three years ago, he mounted two devices, a few hundreds of meters apart, on Tokyo’s iconic Skytree broadcasting tower and connected them with a fiber link. After six months, he showed that the highest clock was ticking 4 nanoseconds faster per day, detecting changes in time due to gravity.

The finding supported Einstein’s work while demonstrating that ultra-precise timekeepers could operate in the field. Katori and team are now developing a network of optical lattice clocks across Japan to monitor the Earth’s surface.

Such activities have spurred transportable clock development across the rest of the world, including Europe. Schreck, for one, is keen to find out what will come next. “[With AQuRA], we’re really aiming to take the performance of transportable clock technology to a similar level as existing clocks that occupy an entire laboratory,” Schreck said. “A transportable clock such as this will become really interesting.”
Schreck and his University of Amsterdam colleagues also plan to launch a startup to commercialize the clock-related micro-optics they are developing for AQuRA. “We have the ambition to make all of our technology commercially available, and it would also be cool if our company partners could pick this up and make a product,” Schreck said.

Along the way, the AQuRA team—including researchers from Poland’s Nicolaus Copernicus University, Germany’s Physikalisch-Technische Bundesanstalt (PTB) and France’s Centre National de la Recherche Scientifique (CNRS), as well as industry participants—are working hard on the clock’s vacuum chamber and accompanying lasers. For example, atomic clocks are sensitive to environmental electromagnetic radiation, but the real killer is blackbody radiation: Thermal photons within the clock chamber interact with atoms, altering frequencies and the tick rate. So the partners are developing a temperature-stabilization system to combat this effect. At the same time, a shift from laser diodes to fiber lasers is set to raise overall clock stability.

Critically, such developments will take the AQuRA clock performance beyond the $1 \times 10^{-16}$ level achieved by iqClock. Once built, the clock will be put through its paces at the underground Modane particle physics laboratory in the French Alps. There, it will be fiber-linked to a reference clock at the CNRS lab in Paris to compare its performance. As Schreck noted, this will be a truly testing time; significant differences in gravitational potential between the underground Modane lab and CNRS mean they will be able to assess just how close to the landmark $10^{-18}$ their prototype is.

**FARTHER AFIELD**

Schreck and his AQuRA colleagues are not alone in their endeavors to build a solid supply chain for portable atomic clocks across Europe. “In the U.K., we’re going to be doing exactly the same” with respect to the supply chain, said Ian Hill, lead scientist for the optical lattice clock project at the U.K.’s National Physical Laboratory (NPL). “Sovereign capability and resilient supply chains are all hot topics. We need [portable clock] systems to be transferred into industry, so U.K. industry needs a supply chain for all types of subsystems and components.”

Hill pointed to NPL’s incredibly vibration-resistant, cubic-cavity technology, primarily designed for compact, satellite-based optical clocks but suitable for any portable optical clock package. “There could be a U.K. company that wants to build this subsystem,” he said. “It will be hugely important to have a robust supply chain that feeds into this.”

Hill has been working on strontium optical lattice clocks for years: The NPL-Sr1 that he and his colleagues developed is the first optical clock to contribute to International Atomic Time. He is also keen to get these systems out of the lab. “We don’t want [optical clock] technology to be limited to a very few high-spec labs,” he said. “We want to make this technology translatable, deployable and available to whoever needs this kind of timing capability.”

With that in mind, NPL and its German counterpart, PTB, recently hosted a portable optical clock experiment as part of the ICON (International Clock and Oscillator Networking) project. The program, led by U.K. quantum clock researcher and University of Birmingham professor Yeshpal Singh, is exploring how world-leading transportable optical clocks can be best networked for practical applications.

In the latest experiment, transportable clocks from the Riken Institute and PTB were compared both against laboratory systems at NPL (to validate performance) and against distant clocks via a 2,200-km optical fiber link between NPL and PTB, Hill said. Data from the experiment, which was repeated at PTB, is still being analyzed, but the results are set to nudge portable clocks closer to real-world capabilities.

In the meantime, Singh, Hill and NPL colleague Patrick Gil have just embarked on an £800,000 ($953,000) government-funded project to develop a portable strontium lattice clock over the next two years that they hope will achieve competitive performance in a package 3× smaller than existing transportable systems. And this may come not a second too soon.

To protect national infrastructure from potential satellite systems failure, the U.K. government is investing £36 million in a timely alternative: the National Timing Centre, which will comprise a network of geographically distributed atomic clocks. In an effort led by NPL, tried-and-tested microwave atomic clocks are currently being established across four sites. But as Hill pointed out, the very latest in optical clock technology could eventually expand this network and further secure future telecom networks, smart grids and other infrastructure that will rely on precise time and frequency signals.

Beyond national security, Hill is eager to see portable optical atomic clocks used in geodesy. “Think about the detail and the temporal resolution with which we could map changes in the geoid if we have networks of these systems operating all over the globe,” he said. “We’re just at the beginning of [measuring] dynamics such as the oscillations of ocean waters due to Earth tides, but things could go much further.”

For his part, Schreck would like to use atomic clocks to build a gravitational-wave detector to detect ripples in spacetime at different frequencies to existing infrastructure, such as ESA’s Laser Interferometer Space Antenna (LISA) and the Caltech/MIT-operated Laser Interferometer Gravitational-wave Observatory (LIGO). “We could mount [optical clocks] onto satellites and measure, for example, infrasound gravitational-wave signals,” he said.

“Every time we raise the precision of optical clocks, we can do more physics,” Schreck added. “There are new phenomena hiding behind every next decimal point.”

**Rebecca Pool is a contributing writer for EE Times Europe.**
Quantum computing has seen remarkable advances in recent years, with teams around the world pursuing varied approaches to building quantum computers capable of solving complex computational tasks. One of the key technologies that makes such progress possible is quantum photonics, which uses light particles (photons) to encode and manipulate quantum information. Photonics enables straightforward modularity and networking of quantum photonic chips using standard optical fibers. The approach simplifies the construction of large-scale quantum systems and supports long-range horizontal scaling, similar to data centers or high-performance computers.

Photonics plays a crucial role in the development of quantum computers by offering a solution to secure scalable structures. Photons’ quantum states are robust against decoherence, making them less susceptible to unwanted interactions that could disrupt their quantum state. While photons rarely interact with each other naturally, scientists have devised innovative methods to make them communicate and form multi-qubit gates. One approach involves a photon storage ring and scattering unit, with photons held in a fiber-optic loop and manipulated to interact with a single atom. This interaction creates an entangled state—a fundamental requirement for quantum computing.

Photonics’ advantages include simple components, versatility in running various quantum operations and excellent performance under practical environmental conditions. The technology’s compatibility with existing telecom light sources and silicon chip fabrication methods accelerates progress in quantum computing research. From fault-tolerant quantum computers to a reservoir computer for use at the edge, photonics is being leveraged to power a wide range of quantum computers.

TOWARD A FAULT-TOLERANT QUANTUM COMPUTER
Quantum computing harnesses the principles of quantum mechanics to perform complex computations at unprecedented speeds. Palo Alto, California–based startup PsiQuantum aims to develop and deploy a practical, fault-tolerant quantum computer. Its approach relies on photonic qubits, which are single photons encoded at the 1,550-nm wavelength, propagating within integrated photonic waveguides representing the quantum states 0 and 1. Photonics technology plays a crucial role in generating, manipulating and measuring these photonic qubits using integrated photonic components.

“Quantum photonic chips can be networked using standard optical fiber and without the need for transduction,” said Pete Shadbolt, co-founder and chief strategy officer at PsiQuantum. “This enables straightforward modularity and decoupling of systems, as well as long-range horizontal scaling, leading to a full system that can be modularized and networked with optical fiber, in much the same way as a data center or a high-performance computer.”

PsiQuantum says its fusion-based quantum computing architecture involves generating, entangling and measuring single photons to synthesize a quantum error-correcting code. This architecture requires advanced photonic components, including pseudo-number-resolving single-photon detectors, high-speed multiport optical switches and cryogenically compatible optoelectronic packaging.

“Quantum photonics can, for the most part, leverage existing infrastructure, tools and know-how for high-volume semiconductor manufacturing, packaging and systems integration,” Shadbolt said. “The reliability, throughput and process control that have already been established for commercial integrated photonics applications are hugely advantageous given the scale and complexity of the system required for any kind of fault-tolerant quantum computing, and in our view, this leverage significantly accelerates and de-risks the path to large systems.”

One major advantage of photonics in quantum computing is the compatibility with existing infrastructure and manufacturing processes for high-volume semiconductor production. PsiQuantum said it invests heavily in semiconductor process development for integrated photonics, enabling efficient manufacturing processes. Moreover, photonic qubits have physical properties that make quantum computing advantageous at scale. The use of photons allows for higher operating temperatures, providing more headroom for cooling power, and makes the system immune to certain sources of decoherence, enhancing overall stability.

QUANTUM COMPUTING AT THE EDGE
While PsiQuantum is developing large-scale quantum computers, Virginia-based startup Quantum Computing has unveiled a reservoir computer to handle demanding computational challenges at the edge. The portable hardware device, about the size of a small power pack, aims to make neuromorphic computing...
hardware accessible and affordable to individuals and small businesses. The approach maps input signals into higher dimensional computational spaces using the dynamics of a fixed, nonlinear system called a reservoir. The company says its reservoir computer offers ease of training, high processing speed, power efficiency and the ability to address such challenges as exploding and vanishing gradients in typical recurrent neural networks.

"Unlike classical computers, the reservoir computer achieves computational parity without the burden of high electrical costs during training," said Robert Liscouski, CEO of Quantum Computing. "Its key strengths lie in speed, computing power and the ability to operate at the edge."

The company claims that reservoir computers exhibit remarkable performance in time-dependent tasks, such as chaotic time series prediction, radar signal classification and speech recognition. It predicts that conventional barriers to reservoir computing adoption, including computing costs and technical complexities, will be dismantled with the introduction of its reservoir computer.

Quantum Computing said its reservoir computer requires significantly less electricity (about 80% to 95%) than traditional computers and can interface with host machines through an Ethernet connection. The computer acts as a computing platform for machine-learning-specific tasks, offering expanded dimensionality compared with the original data to yield more detailed insights and reduced training time. The reservoir computer is targeted to be used across various industries, from data analytics and optimization to pattern recognition and forecasting.

"The photonics-based approach is a highly iterative and technically advantageous method," Liscouski said. "Leveraging the inherent capabilities of photonics, such as room-temperature operation, inherent coherence and stable entangled photons, we aim to democratize and widely apply quantum computing technologies. We're introducing these innovations to the market, capitalizing on the fundamental strengths of photonics."

The company recently announced a subcontract award to build and test a photonic sensor instrument for the U.S. National Aeronautics and Space Administration’s Ames Research Center. The instrument will provide NASA Ames with accurate measurement of atmospheric particulates like clouds, aerosols, smoke and volcanic ash. Under a previous subcontract with NASA, Quantum Computing is also leveraging its photonic LiDAR and reservoir photonic computing systems to remotely measure the physical properties of different types of snowpack, including the density, particle size and depth. This expansion into different quantum domains, such as imaging, sensing and cybersecurity, showcases the potential of photonics in quantum computing applications.

WHAT’S NEXT FOR PHOTONICS IN QUANTUM COMPUTING

Photonics holds huge promise for realizing the full potential of quantum computers. While still in its early stages, the technology could address the challenges of scalability and decoherence, crucial for building fault-tolerant quantum computers and for bringing quantum computing to the edge.

Different teams are exploring a wide range of potential use cases, including financial applications, machine learning and optimization. As progress in photonics continues, we can expect to see robust quantum error-correction techniques and the realization of commercially valuable applications in areas like chemistry, materials science, energy and healthcare.

Saumitra Jagdale is a contributing writer for EE Times Europe.
n today’s digital data-intensive environment, the demand for high-performance computing (HPC) continues to surge as organizations confront massive workloads and complex data-processing challenges. New approaches for efficient, high-bandwidth, low-latency compute are crucial for handling these demands as traditional technologies reach their limits in data volume, speed, energy efficiency and footprint.

Data centers are central hubs for large-scale data processing and storage. HPC plays a pivotal role in these environments, requiring efficient and high-bandwidth communication for managing the massive influx of data. Photonic technologies, leveraging light for compute instead of electricity, are emerging as a groundbreaking solution to address scaling issues and improve communications at the data center for HPC workloads.

WHY PHOTONICS?
Photronics is a cutting-edge technology that combines the power of light with the efficiency of silicon to enable low-latency, high-speed computing, data interconnect and transmission, and communication. It leverages the inherent advantages of silicon-based fabrication processes, seamlessly integrating photonic components with electronic circuits on a single package and scaling beyond copper interconnect while delivering superior performance.

The key components of a silicon photonic system include light sources, modulators, detectors and optical waveguides. Laser light sources generate photons that are guided through the waveguides, and modulators control the properties of the guided light, allowing for the encoding of data onto the optical signals. Photodetectors convert
Using Silicon Photonics to Accelerate HPC Workloads

By utilizing light-based transmission, silicon photonics surpasses the limitations of traditional copper-based interconnects, significantly reducing latency and enabling real-time data processing.

Speed is crucial for HPC workloads. Silicon photonics enables unprecedented data-transfer speeds and is ideally suited for data centers, bringing benefits for handling HPC workloads that require faster data-transfer speeds, better energy efficiency and lower latency. By utilizing light-based transmission, silicon photonics surpasses the limitations of traditional copper-based interconnects, significantly reducing latency and enabling real-time data processing.

HPC workloads are also notorious for their high power consumption, resulting in increased operational costs and environmental impact. Here again, light-based computing poses an advantage: Because photons require less power than electrons to transmit data, photonic solutions lower costs and advance sustainability by minimizing carbon footprint.

HPC workloads heavily rely on accurate and reliable data transmission. Silicon photonics offers enhanced signal integrity by minimizing signal degradation and electromagnetic interference. The use of light-based transmission ensures data integrity throughout the communications process, enabling precise and reliable results for HPC computations.

Potential use cases for photonics to accelerate HPC workloads include rack-to-rack interconnect, memory and storage acceleration and intra-chip communication:

- **Rack-to-rack interconnect:** HPC systems often consist of multiple compute nodes interconnected within a data center. Silicon photonics can be used to create high-speed and energy-efficient interconnects between these nodes. Optical links can transmit large amounts of data at high speeds over longer distances with minimal latency and reduced power consumption compared with electrical interconnects. This enables faster communication and data transfer between compute nodes, facilitating efficient parallel computing in HPC clusters.

- **Memory and storage acceleration:** HPC workloads often involve intensive data access and storage operations. Silicon photonics can be employed to enhance memory and storage performance in HPC systems. By leveraging standard interconnect protocols like Compute Express Link (CXL) over optics, the communication between processors and memory/storage subsystems can be significantly accelerated, reducing latency and improving overall system throughput. This is particularly beneficial for large-scale simulations, big data analytics and machine-learning applications, in which rapid data access and processing are crucial.

- **Intra-chip communication:** Within a single chip, a photonics-based optical-network-on-chip can be used to enhance communication between the components, such as processors, memory caches, accelerators and chiplets. By integrating photonics into the chip design, high-speed and low-latency communication paths are created using waveguides that reduce data-transfer bottlenecks and enable efficient data movement between different functional units. This can result in improved overall chip performance, especially for complex HPC workloads that require high levels of parallelism and data sharing.

Overall, photonics in the data center holds great potential for HPC workloads by providing high-bandwidth, low-latency and energy-efficient interconnect solutions. It enables faster data transfer, improved communication between compute nodes and clusters, accelerated memory and storage access and enhanced intra-chip connectivity. These advancements contribute to more efficient and scalable HPC systems, enabling users to tackle complex computational problems with greater speed and accuracy.

**Creating a Photonics Ecosystem to Advance Adoption**

To realize the full potential of silicon photonics, it is important to foster an ecosystem of collaboration. Collaboration among industry, academia and research institutions is essential to drive innovation, accelerate the development of photonics solutions and achieve breakthroughs in manufacturing techniques, component integration and system optimization.

Industry-led standardization efforts also foster collaboration and are equally crucial, as they ensure interoperability and compatibility among different photonic components and systems. Establishing industry standards enables seamless integration, promoting a thriving marketplace and widespread adoption.

Adopting this innovative technology requires a collaborative approach to tune the implementation to solve specific HPC workloads. An emerging ecosystem of photonic computing startups creates opportunities to adopt this technology and participate in influencing their roadmaps. To fully harness the potential of photonics for data center applications, HPC operators must effectively navigate the path to adoption to derive the benefits.

Policymakers will need to collaborate to create an enabling environment that nurtures innovation, safeguards intellectual property and addresses potential regulatory barriers. Supportive regulations can incentivize data centers to embrace photonic technologies and accelerate their adoption for HPC workloads.

Collaborative efforts, R&D investments, standardization and regulatory support will pave the way for the widespread adoption of silicon photonics technology. By leveraging the benefits of silicon photonics, data centers can accelerate HPC workloads, fueling innovation in various domains and driving growth.

Hal Conklin is vice president of business development at Lightelligence.
“In my view, the impact of the new standard will be huge,” said Harald Haas, Li-Fi pioneer, chief scientific officer of pureLiFi and professor of mobile communications at the University of Strathclyde, U.K. “We’ve truly opened up wireless communications in the optical domain, which is a big step.”

Haas’s colleague, pureLiFi CEO Alistair Banham, concurred. “To have this IEEE standard is a massive milestone, and people have been really waiting for this,” Banham said. “But Wi-Fi, LTE or 4G, Li-Fi can now interoperate with the most pervasive RF technology on the planet: 802.11.

“This is fantastic, and I don’t think we can underestimate the importance of the new standard,” he added.

FIRST LIGHT
Li-Fi is a wireless technology that uses light rather than radio frequencies to transmit data. It was first demonstrated by Haas in 2011 at a TED Talk, where he showed how a Li-Fi–retrofitted LED bulb could stream video to a computer by modulating its light intensity. Soon afterward, Haas co-founded pureLiFi with research colleague Mostafa Afgani, and numerous Li-Fi deployments and

With an 802.11 spec in tow, Li-Fi is ready to join Wi-Fi and take data transmissions to unprecedented speeds.
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The pureLiFi executives are also certain that Li-Fi will complement Wi-Fi, at least for now. In addition to being set to offer higher data speeds than Wi-Fi, Li-Fi can provide more secure communications, as light doesn’t pass through walls. However, Wi-Fi has a longer range and, thanks to its ability to penetrate obstacles, can deliver wireless connectivity across many rooms.

“Li-Fi is complementary and additive to Wi-Fi and RF technologies,” Banham said. “For example, with the new standard, RF data can now be offloaded onto Li-Fi in busy networks. There’s a whole raft of new applications emerging all the time, and this will create a larger industry.”

Looking further into the future, Haas reckons that Li-Fi will play a key role in indoor wireless connectivity. Mindful that the wireless market needs to access new frequency bands within its spectrum to relieve congestion, he believes one solution is to use RF for outdoor communications and let Li-Fi take the lead indoors. “Use the radio spectrum outdoors for broad coverage; cover your cities and today’s non-connected environments with RF and leave the indoors for light—it’s already there, and it’s secure,” he said.

NEW PLAYERS

Still, pureLiFi is hardly alone in its Li-Fi endeavors. Companies like Velmenni (India), VLNComm (U.S.), OledComm (France) and Zero.1 (based across Europe and Dubai) have developed Li-Fi access points, antennas, receivers and more. Tech giants like Panasonic, General Electric and Philips (as Signify) have also joined the fray. Thanks to 802.11bb, both Banham and Haas are certain that more Li-Fi players will join the market.

Banham is noticing more companies showing interest in Li-Fi technologies and developing their own products and networks. “I can’t say that [the market] is suddenly going to mushroom, but momentum has already been building, and I say bring it on,” he said. “We want to grow this ecosystem and drive the whole market. This is not a saturated market; it is developing and it will ramp.”

Haas also pointed to myriad analyst reports that predict gargantuan growth. For example, U.S.-based Global Market Insights has predicted a compound annual growth rate in excess of 50% in this decade, delivering a US$8 billion market by 2030. Similar figures recently emerged from Technavio (London).

“The markets are huge, and the standard is a catalyst—I expect a big uptake now,” Haas said. “Different vendors can now enter the market and develop the [technologies] that will make the Li-Fi modem interoperable so that, say, a Samsung phone works with an Apple access point. This is so important.”
Photonics for 5G Networks: Opportunities and Challenges

By Stefano Lovati

Most of the services that have emerged with the digitalization of industry and society are compatible with 5G. Each new category of services comes with its own unique business strategy and set of prerequisites. Building service-specific networks is not an affordable option, however, so the telecoms infrastructure must support all service types, delivering on a wide range of requirements and capabilities, including very high traffic capacity, high data rates, reduced latency, massive device counts and ultra-high reliability and availability. The network must be flexible and scalable to enable the network operator to make the necessary investments for establishing the infrastructure and to evolve the network as needed, at acceptable additional costs over the long term.

Traditional wireless communication technologies are needed to meet these demanding requirements. Photonics, the science and technology of generating, controlling and detecting light, has emerged as a potential game-changer for 5G networks.

Sophisticated photonics technologies will greatly facilitate the implementation of 5G network infrastructure. Photonics can enable low-cost transmission and switching systems in various network segments, simplifying the architecture of some of these systems while outperforming electronics in several important areas. By incorporating photonics into 5G infrastructure, we may accomplish faster and more efficient data transmission, paving the way for the development of new applications and services. This article examines the opportunities and challenges of using photonics in 5G networks.

**PHOTONICS APPS IN 5G NETWORKS**

While not all aspects of 5G networks rely on photonics, several key areas exploit the technology to enable faster, more efficient data transmission. Here are some of the main applications of photonics in 5G networks.

- **Base station connectivity:** To provide extensive coverage and capacity, 5G networks rely on small cells and large multiple-input multiple-output (MIMO) antenna systems. The high data throughput necessitates optical connectivity between these base stations. Photonics technologies facilitate efficient data transport between base stations and the network core. The 5G base station, referred to as gNodeB, uses New Radio technology and is a critical 5G radio access network (RAN) component. It communicates directly with the user devices and manages the wireless connections, providing access to the core network.

- **Transmission via optical fiber:** Optical fibers are the backbone of modern communications networks, including 5G. They use photons to transmit data over long distances with minimal loss as light pulses. Optical fibers connect base stations and data centers in 5G networks to ensure high-capacity data transport between network elements.

- **Optical transceivers:** These devices transform electrical signals into optical signals for transmission and vice versa. They are indispensable components in data centers and base stations, enabling high-speed data transmission over fiber-optic connections. Optical transceivers are utilized in 5G networks to manage the immense data traffic between various network nodes efficiently.

- **Free-space optical communication (FSO):** FSO is a line-of-sight technology that employs lasers for optical bandwidth connections. FSO can transmit several gigabits per second of data, audio and video over the air, enabling optical connectivity without the need for fiber-optic cable or spectrum licenses. 5G networks may use FSO for specific applications, such as providing high-speed, point-to-point connectivity between base stations and backhaul connections. Using lasers, free-space optics rely on photonics to transmit data through the air.

Figure 1: A fiber-optics telecommunication system equipped with DWDM cards
Photonics technology opens new performance opportunities for components used in 5G networks. These include:

- **Higher data rates:** Photonics enables data transmission via optical signals, which have substantially greater bandwidth than the traditional radio-frequency signals used in earlier generations of wireless networks. Photonics components can increase data rates, enabling 5G networks to manage the massive demands of modern applications like virtual reality, augmented reality and ultra-high-definition video streaming.

- **Efficiency:** Photonics offers a more energy-efficient alternative to traditional electronics-based communication systems in light of the growing concern for sustainability and energy consumption. Optical communication uses less energy than conventional electronic systems, reducing the 5G network's energy footprint.

- **Speed:** Photonics enables extremely rapid transmission speeds, minimizing data-transmission latency.

- **Real-time capability:** Consequently, 5G networks can support real-time applications, such as remote robotic surgery, autonomous vehicles and immersive entertainment, where even minor delays can have severe consequences.

- **Scalability:** Photonics’ scalability will make it easier for the 5G ecosystem to accommodate the exponential growth of connected devices and users. Photonics systems can manage additional traffic more efficiently than electronics-based systems as the user base increases.

**Photonics technology opens new performance opportunities for components used in 5G networks.**

**IMPLEMENTATION**

The first challenge is the substantial cost of integrating photonics into 5G networks. Advanced photonics components and infrastructure require significant investment, hindering extensive adoption, especially by smaller service providers and developing regions.

Second, industry-wide standardization is required to ensure the interoperability and seamless integration of photonics technologies within 5G networks. Developing and implementing standardized protocols may require time and collaboration among various stakeholders, such as telecommunications companies, equipment manufacturers and regulatory bodies.

Moreover, photonics and conventional electronics have distinct physical properties and manufacturing processes, making their integration difficult. Extensive research and engineering are required to develop hybrid systems that incorporate the advantages of both technologies without sacrificing efficiency.

Optical systems are also frequently susceptible to the effects of temperature fluctuations on their efficacy. Temperature fluctuations can be substantial in outdoor environments, and maintaining stable photonics operation under varying conditions is a challenge that must be addressed. Although optical signals can transmit data over great distances, their range in free space is significantly less than that of RF signals. This constraint could necessitate a more concentrated deployment of optical transceivers and infrastructure in 5G networks.

**INTEGRATED PHOTONICS**

Integrated photonics technology is an emerging technology based on photonic integrated circuits (PICs), i.e., devices on which several optical and electronic components are integrated. PICs are processors whose data and energy carriers are photons. Compared with electronic integrated circuits (ICs), they offer greater miniaturization, faster processing rates and reduced power consumption. The most widely used materials for building these types of circuits are silicon nitride (SiN), indium phosphide (InP) and silicon phosphide (SiP).

Although 5G communication can be achieved using electronic processors, PICs offer greater bandwidth and link gain than their electronic counterparts. For on-chip delay lines, the phase delay is independent of frequency, allowing each antenna element to be precisely controlled. Considering that the RF signal is converted to an optical signal on the chip, it is simple to accomplish broadband gain by integrating optical amplifier elements.

In this context, the European research project Teraway envisions the deployment of optoelectronic mobile network nodes in unmanned aerial vehicles (drones), an innovation made possible by using integrated photonics. Teraway is a Horizon 2020 (H2020) 5G-PPP Phase III project to develop a disruptive generation of photonics-enabled terahertz transceivers for use in high-capacity backhaul and fronthaul links in 5G networks.

A terahertz transceiver developed by Phix for the Teraway project is shown in Figure 2. It includes two motherboards, one for the transmitter and one for the receiver, that combine the best properties of multiple integrated platforms.

Photonics offers several opportunities for 5G networks, including higher data rates, reduced latency, increased energy efficiency and enhanced security. The successful incorporation of photonics into communications networks could pave the way for the next generation of ultrafast and dependable wireless communications technologies as we progress into the 5G era. To truly realize the potential of photonics in 5G networks, cost, standardization, integration, temperature sensitivity and limited range will need to be addressed.

With sustained research, collaboration and innovation, photonics and 5G can potentially transform how we connect and communicate in the future.

Stefano Lovati is a contributing writer for EE Times Europe.
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The communications industry has an I/O bottleneck problem. When data is unable to be moved into or out of a chip or chiplet at a rate that matches or exceeds the rate at which processing occurs, a backlog is created in the data stream, such that processing/storage conducted in other chips or chiplets is stalled while they await the data. The I/O bottleneck has implications for power consumption in that a significant portion of the power that should be spent on computation and processing is instead used to push data through the system. This is a significant problem for systems that deal with large amounts of potentially unstructured data but that require low latency to function, such as natural-language–processing algorithms.

A disadvantage of advancing technologies is that, sooner or later, the issue becomes unavoidable if further progress is to be made. Such is the case for electrical interconnects, in which chip and package densities have become small enough—and applications demanding enough—that electrical interconnects are reaching the end of their scalability; the detriment to performance is becoming unavoidable.

Optical interconnects are presented as a solution to these performance issues. Using light as the data signal between chips allows for higher-bandwidth transmissions than for electrical interconnects because photons (the quanta of light) are massless and thus do not experience resistance in the same way that electrons do. While photons can be lost via material absorption, scattering with the waveguide and other effects, those occurrences can be mitigated through a careful choice of materials, enabling optical interconnects’ data-transmission rates to exceed those possible with electrical interconnects.

Chip manufacturing—encompassing all of the steps necessary to imprint integrated-circuit designs on semiconductor wafer—is an established process that has been optimized to minimize materials losses, manufacturing time and equipment degradation. The use of chip-to-chip optical interconnects requires a change to this process.
because it requires conversion of the electrical signal to an optical signal at the chip-edge I/Os. This would typically be achieved by incorporating lasers or LEDs into the process—an action that requires consideration of the current required for correct functioning (the lasing threshold for lasers), in addition to whether any other optoelectrical components are required. The inclusion of optoelectrical components into a nominally electrical workflow is a significant change that is reflected in the incurred developmental costs.

Fortunately, developments in several areas promise to lower the barrier to optical interconnect adoption by reducing costs. The relaxing of alignment tolerances is one key way of lowering costs at the assembly stage. Companies working on technology to enable this include Avicena, which is using multimode fibers rather than single-mode fibers (the tradeoff is that you would have to use LEDs rather than lasers), and Teramount, which uses micro-optical elements it calls PhotonicBumps to allow for vertical coupling (rather than coupling at the edge of the die).

In another vein, an increased throughput-to-power-consumption ratio presents savings for the end user. Here, a move to dense-wavelength-division multiplexing (DWDM) is seen as instrumental to achieving higher rates of data transmission, as it allows more wavelengths to be transmitted over a single channel. Intel used DWDM via a distributed-feedback laser in a silicon photonics co-packaged pluggable optics module in June 2022. And Quintessent is looking to achieve coarse WDM (CWDM) × DWDM by using quantum dots to realize a comb laser for 32 wavelengths in a single fiber (what would otherwise require multiple tunable distributed-feedback lasers to achieve).

With the progress made in high-performance computing, AI and 5G communications over the past couple of years, a handful of startups specializing in addressing the I/O bottleneck via optical implementations have received significant funding from major players. Chief among these is Ayar Labs, which has developed an optical I/O chiplet built in a 45-nm process by GlobalFoundries. The product, TeraPHY, is able to reach a bandwidth density of 200 Gbps/mm at the time of writing, with a roadmap to achieving 1 Tbps/mm of bandwidth, which would push optical interconnects firmly into the realm of industry-leading bandwidth density.

Major companies like Intel, HP and Nvidia are watching closely as Ayar Labs’ technology is put to the test across various settings, from creating an AI infrastructure using optical I/O to co-packaged pluggable technology. Both Intel and Hewlett Packard Enterprise have invested in Ayar Labs.

**THE EARLY STAGES OF COMMERICALIZATION**

Whether optical interconnects can be truly commercialized remains an open question, given the changes this would bring to the mature semiconductor industry and the need for collaboration within the supply chain.

The view of IDTechEx is that optical I/O will be commercialized but that the use cases will be largely restricted to data center use. This is because edge devices are not yet dealing with the types of compute-intensive workloads that would benefit from architectural disaggregation (in which high-bandwidth memory sits off-package and is connected to compute clusters via optical interconnects so that compute can be effectively deployed and power efficiency optimized). Notable exceptions would be autonomous vehicles and military sensing applications, in which low latency is critical. The benefits of optical I/O become harder to ignore the further down the line one gets for transmission rates and AI models. To ensure cost-effectiveness at higher transmission rates and more complex models, optical I/O is an attractive solution.

Leo Charlton is a technology analyst at IDTechEx.

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In June, the EU launched a €48-million, 3.5-year project to commercialize silicon photonics. Led by silicon chip foundry X-FAB and including big names like Nokia, Nvidia, Ligentec, imec and CEA-Leti, the photonixFAB project will look to drive photonic product innovation forward while laying a clear path to high-volume manufacturing.

Joni Mellin, X-FAB’s product marketing manager responsible for photonics and business development, thinks the project’s timing is right. X-FAB’s foundry has been processing wafers for photonics-related devices across multiple sites in Germany, France and Malaysia for more than a decade, and customer demand for such services is rising—and fast, Mellin said.

“It’s always a little bit of a difficult question, when to start supporting these activities, especially when the market is not yet exactly in place,” he said. “But we’re seeing more and more big companies investing in [integrated photonics] programs, as well as SMEs who have been developing products, now trying to get these into the marketplace.”

Myriad end customers want to develop commercial silicon photonics–related products and are scouting high-volume manufacturing partners, Mellin said. “Integrated photonics has reached a level of maturity where it starts to make sense to install high-volume manufacturing capabilities. The photonics industry had identified this as a roadblock, so we’re working with photonixFAB partners to set up an industrial-value supply chain.”

INTEGRATION ISSUES

Photonic integrated circuits (PICs) combine multiple photonic and electronic functions on a single chip to create fast and energy-efficient devices, but blending these wildly different elements onto a chip isn’t easy. Over the past decade, heterogenous integration methods have been developed to streamline fabrication, but as PICs increase in complexity, such processes have become extremely intricate and not particularly cost-effective.

Given these market developments and to prepare for higher-volume manufacturing, photonixFAB is setting up heterogeneous integration manufacturing lines at X-FAB for silicon-on-insulator (SOI) and silicon nitride (SiN) photonics technologies developed by Belgium-based imec and by Ligentec (Ecublens, Switzerland). In time, the SiN platform will be commercially available through Ligentec.

As part of these activities, components based on indium phosphide (InP), lithium niobate (LNO) and germanium will also be integrated into SOI- and SiN-based PICs. And by the end of the project, each platform will be ready for low-volume production and prototyping at different technology-readiness levels, with a clear pathway in place for high-volume fabrication.
to reduce packaging costs, while Phix Photonics Assembly (Enschede, Netherlands) will scale up PIC packaging processes for volume manufacturing. Critically, major application developers Nokia, Nvidia, Aryballe, Brolis Sensor Technology and PhotonFirst are on board to test PICs in use cases like datacom and optical switches and infrared spectrometry for consumer healthcare.

**BOLD MOVES**

What is clear from the plans laid out by photonixFAB is that the pieces for an industrial-scale integrated photonics supply chain are being carefully put into place—and some might add that it’s about time. It’s no secret that both the U.S. and Asia are a step ahead of Europe on commercial PIC processes. As Mellin put it, “Europe is excellent in investing in basic research, but traditionally, we have not been the ones to successfully commercialize our results.”

The X-FAB product marketing manager noted that European players had been ahead of the pack on semiconductor development, but then manufacturing largely shifted to Asia. “This has perhaps motivated EU decision-makers and member states to provide incentives and programs for a [PIC] industrial value chain in Europe, which is what photonixFAB is all about,” he said. “[With this], our customers won’t need to go to the U.S., China or elsewhere in Asia to get their chips made.”

Indeed, looking beyond the end of the project, Mellin is confident that partnerships will continue to form, enabling the PIC marketplace to flourish.

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Along the way, Belgium-based photonic IC design software developer Luceda Photonics will establish mature process design kits for the SOI and SiN technologies and will work with Smart Photonics to enable design for the heterogenous integration of InP chiplets and LNO materials. Luceda Photonics will also develop PIC assembly design kits to reduce packaging costs, while Phix Photonics Assembly (Enschede, Netherlands) will scale up PIC packaging processes for volume manufacturing. Critically, major application developers Nokia, Nvidia, Aryballe, Brolis Sensor Technology and PhotonFirst are on board to test PICs in use cases like datacom and optical switches and infrared spectrometry for consumer healthcare.

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Leti Innovation Days was held in Grenoble, France, June 27–29. Keynotes and exclusive interviews with research leaders made it clear that silicon photonics is an area of interest. As an institute for applied research, Leti takes pure research likely to impact the industry and pre-industrializes it, which usually involves developing supporting tools and methods to allow industrial players to integrate the innovation into their applications in ways that enable mass production.

**PHOTONICS**

Leti Develops Optical See-Through AR and MR Systems

By Pat Brans

Most of CEA-Leti display program manager François Templier’s work involves going outside of the organization to see what’s happening with display systems in the real world, but Leti Innovation Days presents an opportunity for Templier to tell the industry what his team is working on. Optical see-through systems, used by both augmented-reality (AR) and mixed-reality (MR) applications, are a key focus, he told EE Times Europe at this summer’s event.

While AR and MR both involve adding digital information on top of real-world images, the digital information displayed by an AR system does not depend on the real-world images. For example, a driver may see video images of the environment behind the car and an “R” superposed on the video to indicate that that car is reversing. In the case of MR, there is a relation between the digital information and the environment. For example, a game might show the real world with a cartoon character hopping around within the scene.

“To make this work, you need additional components to interpret your environment and then place digital information appropriately onto the real world,” Templier said.

Several approaches for optical see-through systems are already available on the market today. The main one involves the use of waveguide technology consisting of a microdisplay, an optical guide and lenses. The real-word image and the synthetic image are coupled in the waveguide and then directed to the point where the coupled image is to be displayed in front of the eye.

“This approach is already quite good,” Templier said. “One important aspect is that it’s compact, which is what’s required for most applications. But what would be even better is if the system could be even more compact.”

**RETNAL PROJECTION SYSTEMS**

Over the past year, Leti has developed a series of retinal projection systems, which cast light onto the user’s eye to scan the retina.

Retinal projection systems help the eye reproduce an image in an optimal manner—and can improve on traditional waveguide technology to couple real images with synthetic ones. Four main components are needed for a retinal projection system to couple images: a laser source, a waveguide, a hologram and a “bridge” between the waveguide and the hologram.

“To activate the image, you need to take light from the hologram, which serves as a kind of reflector,” Templier said. “You need electro-optical activation at the points where you want the light from the waveguide to be reflected on the hologram and projected onto the eye. This bridge between the waveguide and the hologram uses

Pat Brans is a contributing writer for EE Times Europe.
The Electronic Nose Knows—Thanks to Silicon Photonics

By Pat Brans

Based on photonic sensors, a reliable electronic nose is already solving a range of problems in the industry.

One of the advantages of silicon photonics is that multiple sensors can be placed in parallel on a piece of silicon, creating a configuration suitable for pattern recognition. Each of the sensors detects a different aspect of what is being measured, thereby producing an aggregate “fingerprint” that can be compared with a database of known objects.

These compact, low-cost systems provide a suitable platform for electronic nose products. Aryballe, founded in 2014, is a company that develops and markets such products. "It wasn’t until 2017 that we realized the work CEA-Leti was doing with silicon photonics could be really useful to us," said Aryballe founder and CEO Tristan Rousselle. "We investigated this with Leti and co-designed a system with 64 MZIs [Mach-Zehnder interferometers] working in parallel."

“One of CEA-Leti’s areas of expertise is in silicon microtechnology,” said Bertrand Bourlon, head of the optical sensors laboratory at CEA-Leti. "Silicon photonics allow us to build miniature integrated sensor systems that deliver high performance at a low cost. They do very well in terms of specificity—how well a system detects something with a minimal number of false positives. Using silicon nitride refractive index sensors, we can detect less than one part per million of certain volatile compounds in the air and less than 1 microgram of biomolecules in 1 milliliter of liquid.”

After designing the system with Leti, Aryballe developed a proprietary module, which it now markets in the form of an electronic nose. A differentiating feature of Aryballe’s approach is that it grafts tiny biosensors onto the interferometer using peptides, which are small protein fragments. This mimics the human nose, which works with a set of proteins called olfactory receptors connected to neurons at the back of the nose. The neurons lead to the brain, which the company also mimics with data analytics.

For pattern recognition, the interaction of volatile compounds and peptides must somehow be transformed into electricity. Leti and Aryballe’s approach uses silicon nitride to conduct light at a known wavelength. When volatile compounds bind to a peptide that is fixed on an array, they produce small perturbations in the light, which are detected by a camera. Each of the 64 points organized in a matrix has a different set of peptides, so each is affected differently by the molecules being measured. The different readings at the 64 points produce a pattern that serves as a kind of fingerprint that uniquely identifies the molecules.

The analytical part of Aryballe’s data is also inspired by human olfaction. When people sniff something, their brains generate a pattern, which is then compared with a set of patterns stored in memory. The company mimics biology by using its own hardware and software to generate hundreds of thousands of records, which are used to train their algorithm to recognize patterns.

**ELECTRONIC NOSE USE CASES**

A well-trained dog still has higher sensitivity than an electronic nose. But a dog can be used only in a limited number of circumstances—and it takes two years to train a dog. The accuracy of the electronic nose can be expected to improve over time—and there are already specific types of industrial problems it can solve.

The first category of use cases concerns flavors for the food industry and fragrances for perfumes and cosmetics. One of the areas of application is to facilitate process control by testing odors during different stages of food processing. "We can also use smells to predict taste," Rousselle said. "What you want is to see the development of aromas—for instance, in fruits and vegetables—which will give a good taste.” Another use case is detecting combinations of perspiration and perfume for quality control.

The second major category of applications concerns “malodors,” which means exactly what it sounds like: stuff that smells bad. "These are places where nobody wants to put their nose," Rousselle said. "Electronic noses are very much appreciated in these situations.”

Another interesting field of application is in the automotive industry. The electronic nose provides a way to verify vehicle cleanliness without using an intrusive camera. An odor sensor is a good alternative for rental companies to quickly detect dirtiness.

There are also human safety and hygiene applications. Electronic noses can be used to identify fire hazards and to detect bad smells from fermentation bacteria.

Finally, on the health front, some diseases can be detected by an electronic nose. Dog noses are often used for this purpose, and they are more accurate. But in some specific cases, electronics beats biology.

"Dogs can detect cancer and Alzheimer’s disease, which we can’t," Rousselle said. "But what we can do very well in the medical field is detect bacterial diseases."
From medical diagnostics to autonomous vehicles and robotics, photonics is transforming how we perceive and interact with our world by enabling cameras that can capture images with an unprecedented level of detail. Using photonics principles like compressive sensing and computational imaging algorithms, these advanced cameras capture multiple low-resolution images from different angles and combine them into one high-resolution image. The resulting imagery showcases how photonics can enhance resolution capabilities beyond those offered by conventional cameras.

MIT researchers have demonstrated the role of photonics in improving medical imaging by employing a laser-induced ultrasound technique to create detailed images of biological tissue without invasive procedures or ionizing radiation exposure. \(^1\) The technique uses laser pulses to generate ultrasonic waves that are detected by optical sensors, allowing for precise visualization within tissues beneath the surface. Photonics-enabled medical imaging techniques like this one hold immense potential for early disease detection, guiding surgical interventions with higher accuracy and monitoring the effectiveness of treatments.

Emerging solutions for automotive and robotics, meanwhile, include TriEye’s CMOS-based short-wave infrared (SWIR) image sensors and Coherent’s solid-state laser diodes. The companies recently teamed up to demonstrate a laser-illuminated SWIR imaging system for applications like front and rear cameras in cars as well as vision systems in industrial and autonomous robots.

**PHOTONICS-BASED SWIR IMAGE SENSOR**

TriEye is bringing SWIR to mass production with Raven, a high-definition CMOS-based SWIR image sensor, and UltraBlaze, an eye-safe SWIR pulsed laser illumination source. “Developed through nearly a decade of nanophotonics research, Raven utilizes existing high-volume fabrication tools to create a scalable and cost-effective CMOS-based sensor with high resolution,” TriEye co-founder and CEO Avi Bakal told EE Times Europe.

UltraBlaze, meanwhile, enables long-range night vision and depth measurement while remaining safe for human eyes, operating at much higher optical power per pulse than traditional visible or near-infrared (NIR) illumination sources, according to TriEye.

These components form the basis of TriEye’s Sedar (spectrum-enhanced detection and ranging) platform, which the company claims delivers HD imaging and deterministic 3D information under all weather and lighting conditions. According to TriEye, Sedar differs from traditional
1,300 nm to 1,400 nm, offers advantages over traditional LiDAR-based systems, including improved signal-to-noise ratio in outdoor environments, higher eye safety (due to reduced light absorption by the human retina) and enhanced visibility through mist or dust.

“SWIR light interacts differently with matter compared with NIR light,” Dahlmann said. “This unique characteristic allows for enhanced visibility through mist or dust, making objects visible that would otherwise remain invisible in the NIR range of the optical spectrum.”

Traditional SWIR-range LEDs are inefficient and offer low optical output power. Coherent claims its laser-illumination module contributes to the expansion of the SWIR ecosystem by providing a compact, reliable and efficient light source that delivers 2 W of optical output.

Coherent and TriEye believe their collaboration will open up new applications for SWIR imaging. In robotics applications, SWIR imaging plays a key role in localization, mapping, collision avoidance and overall safety. Industries can benefit from SWIR imaging to optimize performance and efficiency in farming and construction machinery, while security systems can achieve improved accuracy and reliability.

Efficiency is a critical factor in applications with limited power supply, such as automobiles and robotics. SWIR lasers currently offer 20% to 30% efficiency. Coherent said its priority is to maximize the efficiency of its lasers, improving performance over time as technology advances and the gap with NIR lasers narrows.

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From diagnostics to robotics, photonics is transforming how we perceive and interact with our world by enabling cameras that can capture images with an unprecedented level of detail.

"The Sedar platform enables mass markets to tap into the benefits of SWIR sensing, gaining advanced capabilities that were not previously available to them due to the prohibitive cost," Bakal said. "Sedar is highly customizable and can be tailored to solve sensing challenges in automotive, emerging industrial [applications], robotics and more."

A key consideration for applications in automobiles and robotics is power efficiency. TriEye said it has addressed this concern by ensuring that its Raven CMOS-based SWIR sensor operates at extremely low power levels, rivaling other commercial CMOS sensors. This ensures optimal performance without significantly impacting battery life in mobile systems, according to the company.

Talking about TriEye’s collaboration with Coherent, Bakal said, “SWIR sensing can provide localization, mapping, collision avoidance and safety, allowing us to interact with our environment in ways that we have only imagined until recently.”

**LASER-ILLUMINATED SWIR IMAGING**

In the realm of optical communications, semiconductor laser diodes find their place in data centers and telecom networks, enabling efficient transceivers and optical amplifiers. Coherent, a provider of photonic and compound semiconductor solutions, has partnered with TriEye to provide semiconductor laser diodes tailored for the Sedar platform. The SWIR laser-illumination module addresses the limitations of current LED-based modules, extending the capabilities of SWIR imaging solutions.

Coherent builds its semiconductor diode lasers using gallium arsenide, indium phosphide and gallium antimonide materials to address a wavelength range covering the NIR, SWIR and mid-infrared (MIR) spectra from 750 nm to 3 µm. It offers a range of laser diode architectures, including edge-emitting lasers (EELs) and vertical-cavity surface-emitting lasers (VCSELs).

"We recognize the emerging ecosystem of SWIR sensing, which presents numerous benefits compared with sensing in the NIR wavelength range," said Gerald Dahlmann, senior director of marketing for consumer electronics at Coherent. For example, Sedar, operating in the SWIR wavelength range of 1,300 nm to 1,400 nm, offers advantages over traditional LiDAR-based systems, including improved signal-to-noise ratio in outdoor environments, higher eye safety (due to reduced light absorption by the human retina) and enhanced visibility through mist or dust.

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REFERENCE

**Coherent’s Gerald Dahlmann**

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Striking a Balance: LiDAR Adoption in Automotive Applications

By Xiaoxi He, IDTechEx

**Automotive OEMs are increasingly integrating LiDAR, but performance may not be driving practical adoption.**

In recent years, with the development and progress of autonomous-driving features, the automotive industry has witnessed remarkable advancements in sensor technologies, with one particular innovation gaining significant attention: light detection and ranging (LiDAR), a remote sensing method that uses laser light to measure distances and create precise 3D maps of the surroundings.

LiDAR has a long history that dates back to the invention of the laser around the 1960s. It was not until the 2000s that the technology started to be applied in commercial automotive applications that benefited from the development of 3D LiDAR, which provides 3D information using a beam steering system. 3D LiDAR systems offer advantages over traditional sensing technologies, such as cameras, radar and ultrasonic systems, by providing high-resolution 3D point clouds of the environment, as well as accurate range detection. Existing sensors already provide advances for improving safety. However, LiDAR is still becoming an increasingly popular option for redundancy purposes with different value propositions, in addition to its perception (such as detection, classification, recognition and tracking) and localization functions. This trend can be interpreted from the increasing number of vehicles announced to integrate LiDAR. Table 1 presents a selection of examples.

**FACTORS DRIVING ADOPTION**

Although the initial motivation for implementing LiDAR in the automotive industry was for LiDAR’s unique value propositions to make up for the drawbacks of existing sensors like the camera system—which is also the key information most LiDAR startup companies are trying to convey—the actual current and near-future LiDAR adoption in automotive is not driven by performance, according to research from IDTechEx. The LiDARs chosen by OEMs are not the most advanced, and the actual value these systems can bring is also limited; at least when compared with the cost, the investment is questionable. Of course, there are still benefits that OEMs can gain, such as alignment with the trend, positive promotion, differentiation in the competition and hardware preparation for future software updates. This may deliver different messages as many players are prepared to improve their performance.

Apart from LiDAR performance, many other factors seem to be more important at the moment: costs, reliability, the possibility to pass automotive grade, supply chain, mass-production capability, scalability and ease of integration, to list a few. And these

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**Table 1:** Existing and near-future passenger vehicles equipped with LiDAR (Source: IDTechEx)
processing (Figure 2). The transmitter and receiver modules are also referred to as the transceiver module.

WHERE ARE THE TECHNOLOGIES GOING?
In contrast to other sensors like cameras, radar and ultrasonic sensor systems, LiDAR faces unique challenges, including technology immaturity, higher costs, an unestablished supply chain and a dynamically shifting market landscape. The rapidly advancing LiDAR technologies and markets introduce a multitude of unanswered questions. The technology landscape is crowded with a plethora of options for each component within a LiDAR system, and the available combinations are numerous, as shown in Figure 1.

To make it simple, LiDAR hardware can be divided into four major modules: transmitter, receiver, beam steering and control/processing (Figure 2). The transmitter and receiver modules are also referred to as the transceiver module.

Tremendous efforts have been focused on the beam steering system, as this is a key innovation of 3D LiDAR. Most LiDAR start-ups also tend to emphasize their uniqueness on beam steering systems. However, the beam steering component plays a more important role in the reliability of the LiDAR technology choices.

Figure 1: Possible LiDAR technology combinations (Source : IDTechEx)
and the regularity of point clouds, while the performance parameters of LiDAR, such as the accuracy, detection range and points per second, mainly rely on the transceiver system. The latter also largely determines the LiDAR cost.

We have mentioned that actual LiDAR adoption is affecting technological choices for LiDAR. Below, we use the beam steering technology and wavelength choices as examples.

**TIER 1 SHOWS PREFERENCE IN BEAM STEERING TECHNOLOGY**

The four popular beam steering technologies are mechanical, MEMS, optical phased array (OPA) and flash. There are also players developing other innovative choices.

The 360° mechanical rotating LiDAR mainly appears in the initial development stage, especially for robotaxis. However, the high cost and lack of reliability prevent it from being widely used in the automotive industry. The semi-solid or hybrid mechanical beam steering technologies are gaining more momentum. These are the rotating mirror, MEMS and (Risley) prism. There are products passing automotive grade based on these three technological approaches. Benefitting from the success of Valeo Scala, rotating-mirror technology is becoming favored by many Tier 1 suppliers and OEMs because of its reliability and reasonable cost structure, and it is increasingly selected for at least one-axis scan. Prism has phased out of the game, although it may find position for industrial applications.

A number of companies still select MEMS, but because of the irregularity of point clouds, excessive workload due to the smaller number of lasers and high intensity of output, MEMS mirror performance and reliability are important challenges. Flash LiDAR is a popular choice but mainly for short-range detection. OPA is considered to be an interesting future direction. However, the practical adoption selected readiness over potential.

**905 OR 1,550 NM?**

Laser wavelength selection presents a battle between 905 nm and 1,550 nm. The simple explanation many use is that 1,500 nm operates in a wavelength range that is safe to human eyes, and therefore, you can increase the power for a longer detection range. However, in practice, there are many factors to consider.

1,550 nm has a longer history than many people think, such as its use in high-end surveying and mapping applications. However, this is not due to the longer detection range of 1,550 nm but the smaller divergence angle.

On the other hand, 1,550 nm has stronger water absorption compared with 905 nm, has worse heat-dissipation capability with its lower optoelectronic conversion efficiency and generally lower number of lasers used in the LiDAR, and presents more difficulties for higher integration, such as VCSELs.

In addition to the performance consideration, supply chain maturity and mass-production scale play important roles in the current market structure in terms of laser wavelength, and 905 nm is dominating. "The demand for better performance will lead the future to 1,550 nm" may be wishful thinking. It is also possible that the current investment in 905 nm will drag the gap larger. On the other hand, frequency-modulated continuous wave (FMCW) may change it, and 1,550 nm goes better with FMCW.

**WHAT’S NEXT?**

Compared with several years ago, there seems to be less technology route controversy in LiDAR, especially in mass production and actual adoption. However, that does not mean the battle of LiDAR’s technology route has come to an end. One lesson for LiDAR players is that reliability and cost play an equal role to performance, if not more. Also, further performance improvements should rely heavily on LiDAR transceivers. Higher levels of integration and chipification might be the next focus.

Xiaoxi He is a research director at IDTechEx.
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Silicon photonics promises to enable faster and more energy-efficient computing, helping to extend Moore’s Law for decades by harnessing fundamental properties of light. It’s a compelling proposition, but the current design implementation infrastructure is not sufficient to support this promising technology. Many of the commercial photonic IC design tools are not mature when compared with electronic IC design tools, forcing design teams to develop their own tools in parallel or to inspect circuits by hand. Foundries are upgrading their processes to better support silicon photonics designs, but design implementation innovations are leading the way.

A few examples are in critical parts of the design flow. Mature layout-versus-schematic (LVS) and place-and-route (PNR) tools are lacking for silicon photonics, whereas mature tool flows are available for traditional semiconductor design. This gap will narrow over time as more EDA vendors recognize the silicon photonics market opportunity. For now, however, photonic IC (PIC) designers are doing plenty of hand layout and manual checking as the only option.

Photonics designers also face foundry challenges. The actual physical implementation is immature for silicon photonics relative to electronics. Monolithic semiconductor processes exist whereby silicon transistors and photonic components and waveguides can be manufactured in the same wafer, but such processes are not able to leverage the state of the art in either technology. This forces designers, who seek to optimize the system performance, to implement both an electronic IC (EIC) and a PIC and connect them together in a 2.5D or 3D hybrid package.

That, in turn, leads to the lack of mature 3D packaging technology and back-end-of-line (BEOL) fabrication processes. Stacking PIC and EIC dies on top of each other requires vias to be inserted in the die connected to the substrate to allow for external connections to the top die. This is typically accomplished using through-silicon vias. Various processing methods can be employed, but not all of the approaches for integrating BEOL processes into photonics fabrication processes are mature. As a result, lead times can be quite long and costs high. Once again, however, this will change as suppliers see the market opportunity.

Finally, and most importantly, transitioning to silicon photonics presents a steep learning curve for traditional IC designers. As in all areas of chip design, engineers are in short supply.

Because silicon photonics is a relatively new field, however, there is a challenge to train engineers. From my experience, physical design engineers who have a background in device design and circuit layout seem able to make the transition quicker than engineers who have been running synthesis and auto-place-and-route (APR) tools, as much of the PIC layout must still be done by hand or with customized scripts.

The talent pool will deepen over time. Photonics and optical engineering programs are offered now at select colleges and universities in the U.S. and elsewhere, and these will grow in tandem with the opportunities.

Challenges with an immature implementation infrastructure and untrained engineers are not unexpected, as the field of photonics is only about 15 years old and the commercial viability outside of the transceiver business is only now being explored. Nevertheless, changes up and down the design and manufacturing chain are needed as silicon photonics gains momentum.

Silicon photonics promises to enable more energy-efficient computing, but the current design implementation infrastructure is not sufficient to support it.

Starting with design, the EDA community has a huge role in refashioning the design infrastructure. It can assist by improving the development process and enabling better, more efficient chip design verification. Packaging for 3D ICs also needs more specialized metrology tools.

Foundries can streamline manufacturing by reducing cycle times and building a more predictable process. They could provide more mature silicon photonics process design kits (PDKs) for new technologies and make them open rather than proprietary. Depending on the design, companies are limited in their options and usually need to generate their own PDKs to qualify their test chips.

Even with the current challenges in design implementation infrastructure, silicon photonics is showing promising commercial viability in various applications. It has the potential to enable technologies and applications not possible with traditional electronic circuitry and to improve the efficiency and performance of existing technologies.

Ron Swartzentruber is director of engineering at Lightelligence.
Every year (or so), EE Times assembles a list of electronics and semiconductor startups that have the potential to create a lasting impact. The Silicon 100, now in its 23rd edition, is marked by three major trends: high levels of interest in artificial intelligence, a significant surge in Chinese startup activity and an increase in startup formation globally across the breadth of the electronics and semiconductor domain.

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In 2022, at least 33 children died of hyperthermia or heatstroke in the U.S., either because they were left unattended in a vehicle or because they independently gained access to an unoccupied vehicle. In the last 25 years, 942 children have died in the U.S. due to heatstroke, and several thousand children have suffered adverse health effects (Figure 1).

To prevent these tragic outcomes, the U.S. Federal Communications Commission (FCC) and New Car Assessment Program (NCAP) have drafted regulations requiring OEMs to install child presence detection (CPD) systems in new cars.

Using In-Cabin Radar Solutions for Child Presence Detection

By Sameer Akhtar Shah, Senior Manager of Product Marketing for Automotive Radar Sensors, Infineon Technologies

There are regular reports of children being left in cars. Many adults underestimate how quickly the inside of a car can heat up in the sun and what the consequences are for children. Child presence detection systems based on radar technology can help warn the vehicle user and thereby save lives. How can the technology achieve this today?

Figure 1: Every year, several children die in hot cars.
Cost. Just one radar sensor in the overhead compartment can cover a whole five-seater car, including corner-case areas like the footwells (Figure 3). The fully Infineon-based system concept includes not only Infineon radar sensors but Infineon AURIX™ microcontrollers with the necessary processing power to run the highly efficient detection algorithms. It detects a child alone in the car within seven seconds—faster than the speed required by the regulations. If a left-behind child is detected, OEMs or Tier 1s can trigger an alert/warning to the user based on the CPD information.

Infineon’s CPD system was extensively tested, and the machine-learning algorithms were trained with real adults and children. Corner cases like footwells and non-living objects like water bottles were also tested. This very reliable system avoids false alarms, which would be a nuisance for the car user. Currently, Infineon is working with its partner NOVELIC (see sidebar) on algorithms that can also distinguish between children and pets.

**ADDITIONAL APPLICATIONS WITH JUST ONE SENSOR**

The very high thermal efficiency of radar sensors enables a size- and cost-optimized solution. And beyond that, radar technology allows additional applications with only one sensor (Figure 4). This diversity streamlines the bill of materials and further optimizes cost efficiency.

Infineon 60-GHz radar solutions enable OEMs to deploy such child presence detection systems with very high accuracy (over 99%), combining ease of use with very low system cost. Just one radar sensor in the overhead compartment can cover a whole five-seater car, including corner-case areas like the footwells (Figure 3). The fully Infineon-based system concept includes not only Infineon radar sensors but Infineon AURIX™ microcontrollers with the necessary processing power to run the highly efficient detection algorithms. It detects a child alone in the car within seven seconds—faster than the speed required by the regulations. If a left-behind child is detected, OEMs or Tier 1s can trigger an alert/warning to the user based on the CPD information.

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**To prevent tragic outcomes from children left unattended in cars, the FCC and NCAP have drafted regulations requiring OEMs to install child presence detection systems in new cars.**

This matches the trend in in-cabin monitoring system (ICMS) applications. Yole expects unit sales to continue to grow in the coming years, with a CAGR of more than 50% (Figure 2). This market development is driven by NCAP regulations (such as the adoption of CPD systems by 2025), government initiatives to reduce fatalities and OEMs’ voluntary commitments to improve occupant safety.

**THE NEEDED TECHNOLOGY**

The most promising technology for ICMS in general and for child presence detection in particular is radar, allowing the detection of target objects in the car. By detecting movements caused by breathing and heartbeats, the radar can distinguish between lifeless objects and living beings. Moreover, the classification is easy for adults and children. The sophisticated sensor technology works without direct line-of-sight and through materials, so the design of the interior is not disrupted by visible lens covers or similar gear. Radar sensors are cheaper and smaller than cameras, consume less power and require less processing overhead. Privacy is also protected with radar sensors, as no images are captured.

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Infineon’s CPD solution can be used simultaneously as a seat occupancy detection system. A single antenna-in-package (AIP) sensor reliably detects and localizes all five passengers in a car. Occupant localization combined with classification can be used by
The two automotive AEC-Q100 Grade 2–qualified sensors BGT60ATR24AIP and BGT60ATR24C, which are used in the child presence detection solution, also come from this family of consumer radar sensors. The modular approach creates the most flexible solution on the market. Furthermore, Infineon already has long-standing know-how regarding AIP technology, which the company was the first to introduce to the market with a consumer product. Now, with the BGT60ATR24AIP, the technology is also coming to automotive applications. Tier 1s and OEMs benefit, as they do not have to design any antennas on the PCB. This reduces time to market and R&D efforts on the customer side.

Despite the integrated antenna, the AIP sensor is very compact, at just 8 × 8 mm². Due to its excellent thermal management, the sensor remains cool in operation even without a heatsink, consuming only 50 mW. Together with the AURIX™ TC3xx microcontroller, a single sensor is sufficient to monitor even the footwells.

**AUTOMOTIVE AIP SENSORS**

Infineon has been a recognized leader in automotive radar for many years. Its market leadership, with over 70% market share for 77-GHz radar and with over 100 million units of 24-GHz BSD radar sensors sold, proves the company’s know-how and experience. Infineon is also very successful in the consumer sector with 60-GHz radar, which is used in market-leading smart TVs, smartphones and more.

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The Infineon system enables even more benefits: Intrusion and proximity alerts can be implemented with the same sensor to increase the safety and security of the car. Tier 1s and OEMs can develop an alarm/alert system that notifies the user about unauthorized access within 500 ms—for instance, if a hand enters through a window, the sunroof or the trunk. To react even faster, the car’s immediate surroundings can also be continuously monitored. If someone jiggles the car or tries to break in, an alarm system can be triggered that flashes the headlights or honks the horn to ward off potential intruders.

**CONCLUSION**

Every year, children who have been left alone in a hot car lose their lives. That’s why the FCC and NCAP have drafted regulations that require cars to have child presence detection systems in the future. Infineon considers 60-GHz radar to be the best technology for this purpose. Thanks to its many years of experience in automotive radar, the company has been able to develop a system that can monitor a five-seater car, including the footwells, with a single sensor.
And That’s a Wrap: Hardware Pioneers Max 2023

By Robert Huntley

Hardware Pioneers Max, an annual single-day exhibition-focused event held in London, is fast becoming a popular draw on the European IoT and electronics industry’s event calendar. First held in 2021 and pitched as the event where electronics, embedded systems and IoT connectivity converge, the “Max” exhibition builds on the Hardware Pioneers evening conference series, which commenced in London in 2014 and later expanded into Germany and the U.S. This year’s Max drew exhibitors from China, the U.S. and Japan, establishing it as an international event.

EE Times Europe caught up with Hardware Pioneers Max co-founder and director Fabiano Bellisario during the show to learn about the event’s evolution to date and its planned direction for the future. “Since 2021, we’ve had good numbers of exhibitors that keep coming back,” Bellisario said. “They continue to trust us, and word is spreading about how successful the show is. We focus on connecting people across the industry so they can have meaningful conversations, essentially connecting the exhibitors with the right audience.”

The exhibition floor was bustling throughout the day, and there was standing room only at many of the two companion conference streams’ sessions. The event hosted 80 exhibitors and roughly 2,000 registered visitors this year.

“For 2024, we’re keeping the same venue but moving to a much larger exhibition area to accommodate 100-plus exhibitors and an even larger audience and making it a one-and-a-half-day show,” Bellisario told EE Times Europe.

ELECTRONICS, EMBEDDED SYSTEMS AND IOT CONNECTIVITY CONverge

The event covers the full scope of developing, manufacturing and operating an IoT device. The show appeals to a broad engineering audience, from those with an idea for a product but needing more skills to design it to developers facing specific technical challenges. Conversations with exhibitors made it clear that bringing an IoT device to market requires a plethora of skillsets, and even the most experienced embedded development team will need to call on experts to help them with certain aspects of their design.

The two conference streams provided a total of 20 presentations covering a mix of technical topics, such as ultra-low-power AI at the edge, how to select sensors for condition-monitoring applications and implementing wireless connectivity. Here is a roundup of key topics that caught our attention at the show.
THE COMPLEXITIES OF COMPLIANCE AND CERTIFICATION

Achieving conformance to regional and national safety standards often confuses device manufacturers, requiring specialist support for tasks like functional safety, EMC/EMI, electrical safety, and RF and wireless approvals.

"Compliance is often a last-minute decision for many development teams—something that they try to avoid rather than something they have to face," Nativ Or, CEO of 360 Compliance (Binyamina-Giv’at Ada, Israel), told EE Times Europe. He encouraged engineering teams to tackle the topic early in the design process to avoid unnecessary costs and significant rework later in the project.

Or said his company offers a turnkey "regulatory testing from start to certificate" service. He stressed the importance of pre-compliance testing and establishing synergy between design and compliance throughout a project’s life.

COLLABORATION SYNONYMOUS WITH IoT

Demonstrating the benefits that collaboration brings to the end user, David Connolly, director of product marketing at Taoglas (Dublin, Ireland), described the company’s cooperation with u-blox (Thalwil, Switzerland) to design a highly integrated, high-precision GNSS module. "The low-power EL20 module incorporates a Taoglas Edge Locate Smart Antenna and a u-blox ZED-F9P module with Multiband RTK [real-time kinematic] to enable centimeter-level positioning," he told us.

“Our active antenna covers the GNSS L1/L2/E5b/B2b bands.”

Connolly said the collaborators had recognized that customers need help with antenna integration, so the module offers an easy-to-integrate approach that speeds time to market for applications requiring high-precision positioning, such as robotic lawn mowers and smart agricultural machinery. Speaking generally about wireless designs, Connolly recommended "integrating the antenna into the design at an early stage as a way of speeding up the development to get to market quickly."

Neil Hamilton, head of growth at u-blox, spoke with us about the company’s cooperation with Taoglas. There has been "a lot more collaboration across our industry," he said, as developers start projects only to encounter "challenges and compromises suddenly. There is much learning on the fly, so collaboration speeds up innovation. You can’t be an expert in everything, so cooperation adds skills and experience." He explained that the u-blox Point Perfect subscription service works with the EL20 module and briefly discussed establishing the business case for asset tracking. He noted that an asset tracker should cost no more than 1% of the asset’s value.

LEGISLATION GIVES SECURITY TEETH

Crypto Quantique (London) was among the exhibitors that focus on securing embedded systems. "People are much more aware now that they must solve the security problem," said director of applications Chris Jones. "You can’t be good enough in security, so we advocate [taking] the best approach rather than accepting anything less. From the Crypto Quantique perspective, end-to-end security starts at the chip level."


DATA SOVEREIGNTY AND ROAMING RESTRICTIONS IMPACT WIRELESS CONNECTIVITY

Several wireless connectivity product suppliers and service providers exhibited at the show. Iain Davidson, senior product manager at virtual cellular network IoT connectivity provider Wireless Logic (Maidenhead, U.K.), spoke with us about the company’s range of global SIM and e-SIM 5G, LTE-M, NB-IoT and LPWAN connectivity, security and IoT device management services. Davidson noted that more network operators are beginning to restrict roaming capabilities and warned of the impact on global connectivity.

Paul Marshall, co-founder of wireless connectivity provider Eseye (Guildford, U.K.), cited the need for more localization, as some mobile network operators restrict IoT devices from roaming, which leads to increased connectivity complexity. "There is an element of maturity when talking to embedded developers about how device connectivity is delivered, with some customers very focused on connection reliability," Marshall told EE Times Europe. "Also, there are different attitudes to using a hybrid connectivity approach, as "more connectivity equates to more cost," which may be untenable for some applications."
Marshall also broached the topic of data sovereignty, commenting, “Some countries are now passing legislation that stipulates any data collected within that nation is kept there. This introduces the need to be able to prove it, requiring the customer to conduct due diligence that it is complying with the legislation.”

LOW-POWER DESIGN STILL DRIVING THE INDUSTRY
Many exhibitors discussed low-power design implementation, approaching the topic from the perspectives of embedded application development, selecting sensor technologies and monitoring a system’s behavior and power consumption profile.

Aleksandr Timofeev, CEO of Polyn Technology (Caesarea, Israel), gave a presentation on achieving ultra-low-power pre-processing of sensor data using the company’s neuromorphic analog signal processing (NASP) front-end IC. “For some sensor applications, 99% of the signal is noise, so pre-processing the data at the edge rather than sending it to the cloud makes sense,” he told EE Times Europe. “Our NASP IC opens the opportunity for a new generation of sensor nodes for real-time AI applications at the edge.”

Placed after the sensor, the NASP IC processes the raw data and sends only useful data onward. Timofeev said that the flow of data transmitted is reduced by a factor of 1,000 and that the IC’s power consumption is less than 100 µW.

Another presentation on low power was given by Matteo Scordino, co-founder of Elimo Engineering. Scordino’s presentation provided insights into some of the techniques and tools embedded developers can use to achieve a low-power design but also suggested that sometimes it’s impossible: “As in many engineering situations, you need to conduct a cost/benefit analysis for low-power design. There will always be tradeoffs between low-power design and the bill of materials.

“Sometimes, if you get within, say, 10% of your [power consumption] goal, squeezing the last microamp out of it might not be worth it except in extreme cases,” he added. “Device usage, battery aging and chemistry variations all have an influence.”

MACHINE LEARNING SPEEDS EMBEDDED SOFTWARE DEVELOPMENT
With the current interest in machine learning, it was only a matter of time before its abilities would be turned toward speeding up embedded development. Michael Lazarenko, CEO of startup Embedd.it (London), spoke to EE Times Europe about how his company uses machine learning to develop device drivers for semiconductor ICs.

“In the future, we believe that the embedded developer won’t need to worry about how the underlying hardware functions,” Lazarenko said. “They won’t need to worry about a particular mode, configurations or how registers in interfaces function. Those interfacing tasks are very manually oriented, and the language of communication between the semiconductor manufacturer and the embedded software developer has been a PDF document for a long time. With the advances in machine learning, we saw an opportunity to structure and understand the PDF data to the point that we can use proven code-generation technologies to abstract from the hardware and help developers integrate new semiconductors into the firmware.”

Lazarenko said the system works “by ingesting the component PDF datasheet to extract essential information like charts, tables and graphs to format it in a specific way to generate a large language model. A structured and editable device driver is generated from this, which provides high-level functions. Rather than going through hundreds of pages of the datasheet, the developer gets a digital component model for, say, a light sensor.”

TIP: CONSULT EXPERTS EARLY IN THE DEVELOPMENT PROCESS
A common theme in the interviews with exhibitors and speakers at the event was the recommendation that developers seek expert advice early in the design process. The nature of the support required will vary according to the project’s specifications and the skills of the team but could cover antenna selection and placement, achieving regulatory and statutory compliance or selecting a global wireless connectivity provider. The benefits of adopting this approach include accelerating time to market and avoiding unanticipated nonrecoverable engineering costs.

Robert Huntley is a contributing writer for EE Times Europe. This article originally ran online at bit.ly/3Yn2oDj.
The RISC-V instruction set architecture (ISA) is one of the most notable contenders to emerge in the ever-evolving realm of computer architecture. Because of its modularity, RISC-V provides more flexibility and customization possibilities than the Arm and x86 ISAs, and it requires no license fees. The open-standard ISA, which started in 2010 as part of the Parallel Computing Laboratory (Par Lab) at the University of California, Berkeley, is now being used in more than 10 billion CPU cores in the market and continues on an aggressive growth path. The main factors that have helped RISC-V attract the attention of researchers, developers and industry leaders are its simplicity, modularity and openness.

**RISC-V’s modularity makes it highly customizable and adaptable, enabling designers to incorporate only the instructions required to implement their solution.**

RISC-V is the fifth generation of the Reduced Instruction Set Computer ISA. At its core, RISC-V employs a load-store architecture, in which data is loaded from memory into registers, operated upon using arithmetic and logical instructions and then stored back into memory. It features a fixed-length instruction format with a variety of base integer instructions, as well as optional instruction extensions for floating-point operations, vector processing, cryptography and other tasks. The ISA is organized into multiple privilege levels, allowing for the secure and efficient execution of software at different levels of the system.

The modularity of RISC-V makes the ISA highly customizable and adaptable to various computing requirements, enabling designers to choose and incorporate only the instructions required to implement their solution. Its open nature and flexible design have made it popular for research, development and innovation in the field of computer architecture.

RISC-V is set to follow the same path as Linux, whose development community has made contributions over the years that...
have expanded the open-standard operating system’s functionality and market. Similarly, developers in the RISC-V ecosystem are working together to create ISA and non-ISA specifications that leverage the advantages offered by RISC-V. Many companies have started developing products based on RISC-V and are targeting use cases from analog intellectual property (IP) and formal verification to GPU vector cores.

**RISC-V–BASED CUSTOMIZABLE VECTOR CORES FOR HIGH-PERFORMANCE COMPUTING**

One such company is Semidynamics, a Barcelona, Spain–based startup that has been pushing the boundaries of vector processing with vector cores. One of RISC-V’s unique features is its ability to offer a high level of customization, especially for vector units. Roger Espasa, co-founder and CEO of Semidynamics, cited RISC-V’s support for variable vector lengths and said the company has taken full advantage of that flexibility to introduce the largest vector unit in the RISC-V market, with a data-path length scalable to a massive 2,048 bits. The company can also implement new instructions at customers’ request, Espasa said. “This extensibility empowers our customers, enabling them to shape the ISA to their specific needs,” he said.

Espasa said RISC-V–based GPU cores could potentially serve as compelling alternatives to existing GPUs, which consist of multiple CUDA cores. A vector unit, comprising multiple vector cores, is directly connected to a fully functional RISC-V core. “This direct connection makes programming a vector unit super-easy compared with a GPU,” he said.

While a competitive RISC-V solution would require a quantity of vector cores that would be similar to the CUDA core count in traditional GPUs, “the increased flexibility and programmability offered by RISC-V–based vector units … could potentially lead to new software ideas that we can’t even think of today,” he added.

Addressing power efficiency concerns, Espasa outlined Semidynamics’ architectural approach. By incorporating 2×, 4× and 8× ratios between vector register bits and the number of vector cores in the unit, power efficiency significantly improves. This is achieved by utilizing the vector unit for consecutive clocks and gating the rest of the pipeline during those periods.

“In Intel’s AVX-512, you need 8× the same instructions to do the work of our 4,096-bit vector instruction,” Espasa said. “This means you need to fetch, decode, rename, issue and retire 8× more instructions on Intel than on our solution. That’s where the power savings come from.”

To facilitate developers in maximizing the potential of RISC-V vector cores, Semidynamics provides support for the standard Linux and GNU software stack. The company says it ensures compatibility with GCC and LLVM compilers to enable seamless integration of its hardware with the existing software ecosystem. While offering some performance optimizations, Semidynamics also aims to eliminate the need for custom/vendor-locked software, providing peace of mind to customers looking to safeguard their software investment and ensure the possibility of future migration.

The Semidynamics vector unit’s ability to enhance data handling in RISC-V cores is one of its notable features. A single vector load instruction can request multiple cache lines, thereby significantly reducing the number of loads required in scalar machines. With the LMUL=8 feature, a single vector load instruction can request 64 cache lines, Espasa said. “Being able to fire so many requests to the memory system is how the vector unit improves the data-handling capabilities of general RISC-V cores.”

Semidynamics’ vector cores are enhanced by a high-performance, cross-vector-core network that facilitates seamless connectivity between the vector cores. This network plays a crucial role in executing certain instructions, such as VRGATHER, VSLIDEUP/DOWN, VCOMPRESS and VEXPAND, enabling developers to write complex algorithms with ease, particularly in vector mode, according to the company.

**FORMAL VERIFICATION APPS TO HELP DEVELOP BUG-FREE RISC-V CORES**

As companies adopt RISC-V for their products, one challenge has been ensuring that their cores are bug-free. Companies are required to invest more in testing and making sure that all possible boundary cases are addressed, which can be a tedious task. One proven method is to use formal verification, an exhaustive approach that mathematically proves the absence of bugs in hardware designs.

Axiomise, a London-based provider of formal verification solutions, says its formalISA app, developed specifically for RISC-V processors, revolutionizes the process of architectural and micro-architectural verification. In an interview with EE Times Europe, CEO Ashish Darbari shed light on the benefits of formal verification and how the
formalISA app reportedly transforms chip development processes.

The app employs a suite of architectural properties, including assertions and covers, which are run against any formal verification tool from leading vendors like Cadence, Mentor and Synopsys. The architectural properties are customized at runtime to probe the architectural signals of the RISC-V implementation, ensuring conformance to the RISC-V ISA.

By leveraging the official RISC-V open-standard specification, the app provides all the necessary architectural proofs to validate the implementation with formal methods, Darbari said. "The formalISA app for RISC-V has been designed by formal verification practitioners from Axiomise," he said. These professionals "have [worked in the] trenches for two decades verifying semiconductor designs with formal verification, so they understand the performance, efficiency and quality aspects of the formal testbenches and the need for automation."

A unique aspect of the formalISA app is its focus on architectural verification, which helps to identify micro-architectural artifacts and optimizations that can introduce bugs. Darbari pointed out that power, performance and area optimizations are a common source of bugs, and the app’s assertion/cover-failure capabilities highlight these issues.

"There is currently no other formal verification solution available for RISC-V that is vendor-agnostic and can provide exhaustive proofs, find corner-case bugs, do intelligent debug and provide coverage and reporting all under one roof," Darbari said. Those features, combined with the ability to work with any formal verification tool, make the formalISA app a game-changer in the field of formal verification for RISC-V processors, according to the CEO.

When asked about the company’s experience with RISC-V, Darbari said, "We love RISC-V because it is open-source, simple and extensible, and there is a rich ecosystem." He said the formalISA app had caught deadlock, functional-safety and security issues in processors including ibex, zero-riscy, CV32E40P and WARP-V implementations.

Axiomise says it has collaborated with some significant players, including AMD, Pulp Platform teams and the OpenHW Group.

Looking ahead, the company plans to enhance the formalISA app, including testbench extensions to RISC-V instructions and further improvements in debugging, coverage and reporting capabilities.

CUSTOMIZABLE ANALOG IP FOR RISC-V SUBSYSTEMS

Agile Analog, a Cambridge, U.K.–based startup specializing in analog IP, now provides analog subsystems designed specifically for RISC-V systems. "Our tagline is, ‘Analog IP the way you want it,’” said Chris Morrison, director of marketing at Agile Analog. "We provide analog IP that can be customized to the customer’s exact requirements."

Morrison emphasized the challenge of integrating analog IP into systems and said that Agile Analog aims to simplify the process for customers. By combining various analog IP elements and wrapping them in a digital interface, Agile Analog ensures seamless integration without interference, enabling customers to treat analog blocks as digital components, he said.

The growing popularity of RISC-V as an open-standard ISA has driven Agile Analog’s interest in developing RISC-V subsystems. Morrison highlighted the significance of analog interfaces in RISC-V systems for tasks like setting voltages, measuring currents and utilizing sensors. The company’s RISC-V subsystem provides customizable analog IP to help customers address those needs.

Agile Analog’s analog IP offerings can be extensively modified, allowing customers to fine-tune such parameters as accuracy, resolution and the number of units. "This level of customization sets Agile Analog apart from other analog IP providers and makes us more capable of delivering optimal solutions aligned with specific power, performance and budget constraints," Morrison said.

When integrating analog circuitry into SoC designs, digital chip designers face several challenges. It is difficult and expensive to find good analog engineers, and additional expertise is required for mixed signals and simulation tools. Agile Analog’s RISC-V analog IP subsystem mitigates those challenges by simplifying analog integration and reducing costs, Morrison said. "It’s all about making analog integration easy. We do all of the hard work and deal with the issues mentioned earlier, and then the digital designer can integrate the analog IP in the same way as they integrate a digital block."

Agile Analog’s verification process ensures the reliability of analog-digital interactions, providing confidence to designers, he added.

When asked about the target market, Morrison said, "The initial RISC-V subsystem is designed predominantly for IoT and battery-powered embedded applications. It’s low-power and has the features that are needed for wearables, headsets or anything that is battery-powered and portable."

Looking ahead, the company plans to develop subsystems to address built-in testing, advanced power management and more sophisticated process, voltage and temperature sensing.

THE FUTURE OF RISC-V IN THE COMPUTING LANDSCAPE

RISC-V has emerged as a game-changing open-standard ISA, revolutionizing the world of chip design and enabling a new era of innovation. Its flexibility and scalability have attracted a wide range of companies, from startups to industry giants, which are leveraging the architecture’s ability to create diverse applications across various domains.

The views shared by industry experts have highlighted the significance of RISC-V, its customization potential and the role of analog IP subsystems in simplifying integration challenges. As RISC-V continues to evolve and gain momentum, we can expect even more groundbreaking developments, driving the next wave of technological advancements and shaping the future of computing.
very year, embedded hardware and software developers face new challenges. Some of these come from industry trends, such as the increasing use of machine learning at the edge. Others are driven by customer and market expectations, such as delivering more functionality in a smaller enclosure with a lower BOM cost. And let’s remember the need for sustainability in design and the increasing legislation covering batteries and battery waste. For developers, keeping up to date with trends takes time, but putting it into practice takes even longer.

As machine-learning algorithms progress toward the edge and demand for functionality increases, embedded systems become more complex. This fact is highlighted in a 2022 article by management consultancy firm McKinsey titled “Cracking the complexity code in embedded systems development.” The article listed many contributing factors, including marketability over engineerability, a topic most engineers know only too well. However, all of the above factors are set against an embedded development process that has remained largely unchanged for decades. Today’s integrated development environments have advanced considerably in the past two decades but still function based on the code, compile and debug cycle.

Nevertheless, the ecosystem of hardware and software tools available to developers is expanding, easing development challenges and opening up opportunities for development teams to increase device functionality. EE Times Europe has investigated three products that may reduce the burden on engineering.

EMBEDDING INSIGHT INTO YOUR APPLICATION

During this year’s Embedded World conference, software company Qt (Helsinki) launched Qt Insight, an insight and analysis application for embedded systems that the company describes as providing real customer insights into the usage of applications and embedded devices. EE Times Europe spoke with Petteri Holländer, senior vice president of Qt Ventures, to find out more about Qt Insight and its suitability for embedded designs.

“In the past, most embedded devices didn’t have any network connection, so the only feedback on user experience that manufacturers could gain was from a focus group, and that was after the fact, when the product was in the market,” Holländer said. “Now, with more connected embedded devices, customers have asked us about collecting user feedback, updating device firmware and even displaying ads on screens. Something we found by running pilot cases with customers—and it’s sort of obvious—is that what the device manufacturer thinks the user workflow will be is not how users are actually using it.

“Imagine a coffee machine used in a chain of coffee outlets,” he said. “How do you know how often they are used and when? Is it busier in the morning or the afternoon? What type of coffee and roast is more popular than others? The coffee machine is a simple example, but you could apply it to, for example, an automotive infotainment system. Now that we’re so connected, it’s about making users happy, updating the user interface and potentially displaying advertising for some applications.”

Holländer cited the ability to “promote the correct usage of a device by monitoring the workflow users took to a particular function and suggesting tips to a user that there is an easier way to get to that function. You can do this interactively and dynamically by advising the user or changing the user experience going forward.”

One reason Qt Insight might be used,
LEVERAGING MACHINE LEARNING FOR EMBEDDED DEVELOPMENT

The embedded industry is awash with use cases for incorporating machine-learning algorithms into IoT devices. However, startup company Embedd.it (London) is working on improving developer productivity by using machine learning to write device drivers.

Embedd.it CEO Michael Lazarenko told EE Times Europe how the company started: "As an embedded developer, what created friction was the language of communication between a semiconductor manufacturer and an embedded developer being a PDF document. We saw an opportunity to use machine learning to structure and understand the data in the PDF and then use some proven code-generation technologies to put things together for the developer. This will help them abstract from the hardware, which would also help them port to another semiconductor firmware."

When asked whether developers may be concerned that they no longer have visibility of the low-level functions, Lazarenko said, "We give full transparency of the data that's going into the driver, and we also provide them full access to the source code. From what we are seeing, there is still at least 20% of the development time to be allocated to driver development, but we can speed up that process by 80%.

"Also, we don't just generate the driver code; we create test suites the developer can use," Lazarenko added. "It's a C application that emulates the component's behavior, and you can run it on physical hardware. So that means not only do we generate the driver, but you can also significantly speed up debugging since you have test code already written."

Lazarenko gave an example of a Wi-Fi module he had previously worked on that had a mistake on the datasheet, taking him a month to debug the driver. "We want to address this challenge," he said. "It's about making the whole process of hardware-to-software connection seamless."

Robert Huntley is a contributing writer for EE Times Europe.

Three Tools to Speed Your Embedded Development

minute. "Compared with three years ago, it's better, but I think we are still far from what some of our customers are doing today," she said. "Some are really thinking through the whole development phase, the whole stack in a sense, with a low-power mindset. Many customers are involved in metering, monitoring and tracking [devices], and they have realized that you can't change the battery too often."

Samuelsson referred to companies selling the whole package, meaning an expensive device and monitoring application: "You can't go back in two weeks and say, 'Hey, we need to change all these batteries.' Consequently, they have in their mind that they need to deliver a guaranteed battery life, which is scary. We are seeing more and more customers making energy profiling and prolonging battery life a big deal. This is because they are tired of the firefighting at the end of the project. If you don't optimize the design, it will bite you later, especially since all the projects are multidisciplinary."

When asked what advice she would give embedded developers, Samuelsson said, "The No. 1 things are trying to have a bit more of a bird's-eye view of the project and to keep measuring. The second would be to understand what possible changes could happen during the project and after it is launched. If you have brought the most beautiful low-power product to market and you push out an over-the-air software update that doesn't take care of everything you did in the previous profile, it will ruin everything. Make sure you measure the update's power before it goes live, and get everyone else on the team to measure it and give feedback. I think this also makes the development more of a team play."
The electronics industry is at an inflection point and needs to define new compute trajectories for energy efficiency. As part of EE Times’ 50th Anniversary celebration, this eBook looks beyond silicon to explore advanced materials, design and manufacturing technologies.

Visit the EE Times Store to get your free copy. www.eetimes.com/shop
How Quantum Computing Can Help Make AI Greener

By Román Orús, Multiverse Computing

Picture a world where artificial-intelligence systems operate on the same energy budget as a butterfly. It’s a dream that seems light years away when we look at the gargantuan energy appetite of today’s AI systems.

These powerful machines, as fantastic as they are, swallow electricity at an alarming rate. A single AI model in training can consume as much energy as five cars in their lifetime. Training the last GPT-4 system with all the text from the internet amounted to more than US$100 million in electricity, and it still doesn’t speak well.

It’s not just the training that is costly. One data scientist estimated that in January, the large-language model used as much electricity as 175,000 humans. The training phase is often the most energy-intensive time for AI models, but the intense interest in using these services may create high electricity bills indefinitely.

This problem is becoming even more dramatic, as the demand for AI services is skyrocketing, and the environmental toll is becoming too steep to ignore. We stand on the precipice of an energy crisis, and it’s clear we need to change course.

Are we going to burn the planet with AI? Well, we should have a look at how nature does it. Nature, in its quiet and elegant way, performs computations every moment with remarkable energy efficiency. From a tree converting sunlight into food to the human brain processing complex information, nature’s computations are both sophisticated and sustainable. If nature can do it, why can’t our machines? Clearly, our current approach to AI is fundamentally flawed.

Fortunately, a ray of hope lies in the realm of quantum computing. This emergent field harnesses the principles of quantum mechanics to perform complex calculations far more efficiently than classical computers. Just as nature uses quantum effects in photosynthesis, we could leverage quantum computing to run AI systems on a fraction of the energy.

**POWER CONSUMPTION IN HIGH-PERFORMANCE COMPUTERS**

As AI models continue to grow in both overall numbers and in usage, it’s worth considering the energy required to power the machines that run these algorithms.

The electricity bill for Frontier, currently the world’s most powerful supercomputer, is US$23 million each year for 21.1 MW. When the engineers at Oak Ridge National Laboratory in Tennessee were building Frontier, office space around the computer had to be converted into power substations to ensure the computer had enough energy. Even when it’s idle, Frontier draws 8 MW. One megawatt typically powers 1,000 European homes.

In addition to gobbling up a significant percentage of the world’s energy, these supercomputers have a significant environmental impact in the form of emissions. In 2022, China had the most supercomputers, at 172, with the U.S. close behind, at 128. Coal is by far the most common energy source in Asia and is predicted to hold that spot for the next decade. In the U.S., coal represents 60% of the overall energy mix. In Europe, solar and wind gained parity with nuclear power for the first time in 2022, but there are only 71 supercomputers in Europe. All this supercomputing is contributing to the greenhouse gases disrupting weather patterns and warming the planet.

Even for research scientists trying to reduce their carbon footprint, the use of supercomputers makes that impossible. A recent study calculated the carbon footprint of astronomers at an Australian university. The average astronomer generated 15 tons of emissions from their supercomputer use alone, far surpassing emissions from air travel and from work at the observatory, both of which were in the single digits.

**IMPROVING AI EFFICIENCY WITH QUANTUM COMPUTING**

Just as the world shifts from gas-powered cars to electric ones, businesses, universities and governments can consider quantum computing to reduce the supercomputing carbon footprint. It’s a promising avenue to make AI not just smarter but also greener.

For instance, current exascale and petascale supercomputers typically require about 15 to 25 MW to operate, compared with the 25-kW typical energy consumption of quantum computers.

Additionally, we are seeing the emergence of quantum-inspired computing—algorithms that mimic quantum processes but are run on classical machines. These offer significant power savings compared with traditional AI systems.

For example, one can improve the memory performance of neural networks through quantum-inspired techniques to create more efficient and superfast networks. These networks can do handwriting analysis, speech-to-text transcription and weather prediction, among other tasks.

When quantum computers reach the fault-tolerant era, researchers could use operations on qubits as the artificial neurons in neural networks.

Meanwhile, thanks to quantum-inspired techniques, companies could run networks with a huge number of neurons per layer, with a minimal energy cost, therefore dramatically reducing energy consumption.

One reason high-performance computing centers are interested in quantum computing is because of the opportunity to reduce overall electricity use. As classical supercomputers get more powerful, their power consumption scales almost exponentially. The compute power of quantum machines scales exponentially, but the associated power use scales linearly.

There is some debate about the potential for quantum computers to consume less energy than classical computers. The supporting infrastructure has significant power requirements, with some hardware designs.

The Quantum Energy Initiative, which gathers 300 participants from more than 46
With the rapid growth of connected devices and the internet of things, security has become a significant concern for businesses and consumers using these products. Manufacturers and device vendors are having to respond not only to customer pressure but also to government legislation around the world.

As an indication of the latter, only last month, the U.S. government announced a national IoT security label that manufacturers and retailers can opt to use to assure consumers that their smart, connected IoT devices meet a certain level of cyber safety and are thus less vulnerable to cyberattacks. The new U.S. Cyber Trust Mark program proposed by the Federal Communications Commission (FCC) would raise the bar for cybersecurity across common devices, including smart refrigerators, smart microwaves, smart televisions, smart climate control systems and smart fitness trackers.

Several major electronics, appliance and consumer product manufacturers, retailers and trade associations have made voluntary commitments to increase cybersecurity for the products they sell. The new label supports the IoT security requirements under NISTIR 8425, which resulted from an executive order to improve the nation’s cybersecurity. This label will recognize products that meet these requirements by permitting them to display a U.S. government label and be listed in a registry indicating that the products meet U.S. cybersecurity standards.

Security vendors have been advocating cybersecurity for years and often bemoaned the fact that OEMs weren’t taking security seriously. The emergence of programs like the IoT security label makes their job a lot easier.

One of the companies involved in enabling embedded security in IoT devices is Intrinsic ID. We caught up with CEO Pim Tuyls to get an update on some of the challenges and opportunities for embedded security.

**EE TIMES:** Pim, why is embedded security vital? In particular, what is your company’s role in enabling security in connected devices?

**Pim Tuyls:** Digital trust is one of the world’s biggest problems. Today, everything is connected. And as the number of connected devices grows, touching all aspects of our life, the stakes are higher than ever. Our homes, cars, factories and doctor’s offices are filled with smart devices that constantly exchange information.

Crucially, these devices must ascertain the authenticity of the other devices they communicate with. Similarly to how we establish trust with humans by observing their facial expressions and recognizing their voice, machines also require this kind of trust. How can each machine verify the identity of the other machines it interacts with? This issue looms large in today’s interconnected world, and this is the daunting problem we address.

The foundation of secure systems lies in secure hardware, because trust is virtually nonexistent without reliable hardware. Our specialization at Intrinsic ID is in empowering device manufacturers and chip vendors to develop a robust root of trust through a comprehensive range of both hardware and software IP solutions—all built with physical unclonable function (PUF) technology. PUF tech capitalizes on the inherent variations in the manufacturing process of ICs, enabling the generation of a unique digital identifier.

Specifically, we utilize SRAM PUF, which leverages the behavior of standard SRAM programming to create an unclonable function (PUF) that is used to establish a secure root of trust. This secure hardware, because trust is virtually nonexistent without reliable hardware.

**EE TIMES:** What are your founding technologies at Intrinsic ID?

**Pim Tuyls:** Our mission is to enable digital trust and secure the Internet of Things. We provide comprehensive PUF technology and solutions that help manufacturers and retailers meet and exceed the security requirements of the IoT security label.

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found on any chip to create a unique digital fingerprint. This fingerprint serves various purposes, including distinguishing chips from one another, facilitating secure key generation and storage, device authentication, flexible key provisioning, encryption and efficient chip-asset management.

We’ve been working on commercializing the use of PUF technology for security and authentication longer than any other company. As a result, our technology is in more than half a billion embedded systems and IoT devices, playing a key role in making digital systems more secure.

EET: What specific sectors or applications do you see as the most vulnerable to security breaches, and how can PUF-based security help mitigate those risks?

Tuyls: I’d say all computing applications today need to be highly diligent about security, as semiconductors are everywhere performing important tasks, but one that’s critical is the IoT. The more things are connected, the greater the security risk. It’s estimated that there are 15 billion IoT devices in use today, and that number is projected to grow to nearly 30 billion by 2030.

Each of these devices needs to be secured. The weakest link can be the smallest, simplest sensor or device, where it can be challenging to add security because of the size, cost and the fact that many are already out in the field.

PUF-based security has a big impact on making IoT devices more secure. Using standard SRAM as a PUF, we can deliver a PUF solution via software, which nobody else can currently do. There’s no need to add dedicated PUF circuitry, which makes this cost-effective and scalable for IoT security. A PUF-based software-only solution solves the huge problem of billions of devices that are already connected or that have been developed in the past without security factored in.

In this way, it’s possible for every IoT device to have a unique identity and a hardware root of trust. This establishes a secure foundation for devices and networks and prevents unauthorized access to sensitive data or systems.

EET: In recent years, there has been an increased focus on hardware-based security solutions, such as trusted execution environments (TEEs) and secure enclaves. How does your PUF technology complement or integrate with these hardware-based security approaches?

Tuyls: We are encouraged by hardware-based security solutions, such as trusted execution environments and secure enclaves, because a true security solution involves multiple layers. TEEs and secure enclaves provide a “trusted zone” or a secure and isolated environment within a processor where sensitive operations can be executed securely. This keeps sensitive data secure during execution.

PUF-based security solutions are complementary to these secure environments because they protect sensitive data at rest when it’s being stored. This is because PUFs create the cryptographic keys that are needed to encrypt data outside of the secure environment, either when the data is being stored or when it’s being transmitted.

PUF-based security solutions protect the cryptographic keys they create without needing nonvolatile memory. Traditionally, these keys were stored in fuses or some other form of OTP in the device, so they can’t be changed. However, through invasive attacks, these fuses could still be compromised, which compromises the security of the enclave that’s depending on these keys. With PUFs, this is prevented, as the root secret (and all keys derived from this secret) is never stored. This combination results in a more comprehensive and robust security framework to ensure a resilient digital environment, protecting critical infrastructure, systems and networks in the face of evolving cyberthreats.

EET: The growing use of AI brings both opportunities and security concerns. What are your thoughts on the implications surrounding data privacy and security for this technology?

Tuyls: AI systems require a different approach to security than systems based on traditional IP. In addition to protecting against threats, such as counterfeiting, IP theft and eavesdropping, AI systems must safeguard their data models, which serve as the foundation for AI decision-making. If these models are compromised, the potential consequences are significant, ranging from financial fraud to safety risks in critical applications like self-driving cars.

Furthermore, AI is being deployed both in centralized server environments and at the edge, where devices operate in real-world settings. This distinction implies that different security requirements exist for these diverse deployment scenarios. Edge devices face physical access risks and unique threats that demand specific security measures to ensure the integrity and privacy of the AI systems.

Given the expanding reach and impact of AI technologies, it’s crucial to address security challenges proactively rather than wait for large-scale attacks to occur. And again, it starts at the hardware level. By prioritizing robust security measures, including strong encryption, integrity checks and continuous monitoring, the risks associated with AI can be effectively mitigated, ensuring the responsible and trustworthy deployment of this transformative technology.

**PUF Technology capitalizes on the inherent variations in the manufacturing process of integrated circuits, enabling the generation of a unique digital identifier. (Source: Intrinsic ID)**
EET: Beyond hardware-based security and AI, what other trends or advancements in the semiconductor industry do you find particularly exciting or game-changing? How do you see these developments shaping the future of embedded systems?

Tuyls: As semiconductors continue to play a key role in driving innovation and productivity, the need for a wider adoption of security solutions in 2023 and beyond will continue as well. The data center is one area where security measures are vital. From supporting internet services to driving business operations, data centers are at the core of modern computing and play a significant role in our daily lives.

Digital security in data centers is needed to safeguard the vast amounts of sensitive data, including personal information, financial records, trade secrets and IP, from unauthorized access; maintain its accuracy and reliability; and ensure uninterrupted access.

In sync with high-performance computing comes the need to pack more functionality into smaller form factors, leading to a design trend around chiplets. Instead of designing one big microprocessor with vast numbers of tiny transistors, chip designers are creating smaller chips that are packaged tightly together to work like one system.

Chiplets are combined into system-in-packages (SiPs) to address the growing complexity of chip designs and limitations in chip manufacturing. This provides cost and time-to-market benefits while optimizing functions at different technology nodes. However, spreading functionality across chiplets increases security risks, necessitating robust solutions for protecting component-to-component communications. Because chiplets can come from different manufacturers, ensuring each component is trustworthy is also critical.

EET: Over the last 15 years, since you began your journey with Intrinsic ID, how have you seen the chip-security landscape evolve? And where do you think it will go moving forward?

Tuyls: Over the last 15 years, we’ve seen a tremendous shift in the attitude toward security as embedded systems become more powerful, adaptable and interconnected. Security is no longer an afterthought; it’s now a key requirement for almost all electronic systems. Processors and SoCs increasingly feature hardware roots of trust to handle critical security functions, and security blocks have become common in SoCs. These trends are leading to the next phase of standardization and legislation. In the early days of the IoT, security wasn’t a priority, but that’s changing. Currently, there are industry initiatives focused on putting frameworks in place for IoT security, such as Arm’s PSA and the ioXt Alliance, which are good steps that bring the IoT community together.

PSA Certified is a global partnership addressing security challenges and uniting the technology ecosystem under a common security baseline, providing an easy-to-consume, comprehensive methodology for the lab-validated assurance of device security. As we move forward, addressing the digital security challenges of today and the future will continue to be key to realizing the full potential of a connected world.

EET: Looking ahead, what can we expect from Intrinsic ID in terms of innovation and future product offerings?

Tuyls: With security playing such a vital role in our digital world, it’s a growing market. New security threats will continue to arise, and to stay ahead, we will need to continue to innovate.

New legislation, safety regulations and higher security requirements are driving the need for specialized solutions, and we are addressing this by offering application-specific versions of our hardware product QuiddiKey for key markets, such as the IoT, data center, automotive, and government and defense.

We will also continue to actively contribute to industry standardization efforts. We are working closely with PSA Certified, one of the most important industry-led efforts in standardizing IoT security. Because each IoT device is part of a multi-player supply chain and is used in systems that contain many other such devices, they all need to be trusted and communicate in a secure way. PSA Certified provides a lab-validated assurance of device security.

As digital security gains paramount importance for businesses and governments, we will continue to provide solutions, work with partners and participate in standardization efforts that enable a secure digital landscape.

Nitin Dahad is editor-in-chief of embedded.com. This article originally ran on EE Times at bit.ly/3Ku4wnv.
tinyML will become the largest driver of the microcontroller market in the next 10 years, according to Remi El-Ouazzane, the president of STMicroelectronics’ (ST’s) MCUs and digital ICs group.

“I really believe this is the beginning of a tsunami wave,” he told EE Times in an exclusive interview. “We’re going to see a tsunami of products coming with ML [machine-learning] functionality: It’s only going to increase, and it’s going to attract a lot of attention.”

ST holds roughly a quarter of the MCU market, shipping between 5 million and 10 million STM32 MCUs every day. According to El-Ouazzane, over the next five years, 500 million of those MCUs will be running some form of tinyML or AI workloads.

TinyML, which refers to running AI or ML inference on otherwise generic MCUs, “will become the largest endpoint market in the world,” he said.

El-Ouazzane—who previously served as CEO of edge AI chip startup Movidius and COO of Intel’s AI product group—and his team at ST have been hard at work the last few years using AI capabilities to the company’s portfolio.

“While I believe [tinyML] is the biggest market in the making, I’m also humbly by the fact that we have gone through three to five years of education of management of companies who make fans, pumps, inverters, washing machine drums—all those people are coming to it,” he said.

“We live in the world of ChatGPT, but all these ‘laggards’ are finally coming to use AI. It was my vision for Movidius back in the day. I thought it would happen … It is taking a long time, but we see it coming now.”

TinyML DEPLOYMENTS

Energy-management and automation firm Schneider Electric is using a mainstream STM32 device for people-counting and thermal-imaging applications. To do so, it uses classification and segmentation algorithms on sensor data from a thermal infrared camera. Both the thermal camera pipeline and the AI run on the MCU. Schneider can use the result to optimize HVAC systems, thereby reducing the CO₂ footprint of buildings.

Industrial door specialist Crouzet is also combining STM32 devices with tinyML for predictive maintenance purposes.

“This was interesting because, for them, the cost of maintenance is a huge deal,” El-Ouazzane said. “They have to deploy the maintenance person post-mortem, and if a plane is grounded because a door is malfunctioning ... It is not good news when they receive that phone call.”

Crouzet’s tinyML system can detect signal drift in real time, with high accuracy, to stay one step ahead of a potential failure. The system processes the data in the door and then sends metadata for analysis.

“They are literally changing their business model to be able to deploy maintenance before it is needed, which has allowed them to be way more efficient in how they deploy their maintenance people, and for sure it saves them from receiving a phone call they don’t want to receive,” El-Ouazzane said.

Other examples include Chinese smart-energy company Goodwe, which is using tinyML on vibration and temperature sensor data to prevent arcing in its high-power inverters.

While these are great examples, why are we not seeing the tsunami today?

“Between starting an engagement and [deployment]—after having gone through understanding the platform, prototyping, proof of concept, testing, you name it, and several layers of management approval—it takes three years,” he said. “In the industrial world, it takes three years for a company to start from thinking about something, working with us for the first time, to the library being deployed for production in their product.”

SOFTWARE STACK

In general, ST splits its tinyML customers into two groups. Industrial customers, those with the three-year lead time, generally have little experience with AI, while companies that have invested in data-science expertise can generally turn things around faster. ST takes a similar approach to competitors, including NXP: a software stack that presents different entry points dependent on the user’s level of AI experience.

For the industrial group, NanoEdge AI Studio requires no advanced expertise can generally turn things around faster. ST takes a similar approach to competitors, including NXP: a software stack that presents different entry points dependent on the user’s level of AI experience.

For example, outlier detection might detect a problem, classification might identify the source of the problem and then regression might extrapolate information to provide further insight. NanoEdge AI is used by customers like Crouzet as a low-code platform for working with vibration, pressure, sound, magnetic-field and time-of-flight sensors.

The other entry point, STM32 Cube.AI, allows developers to train neural networks and optimize them for memory- and compute-constrained environments.

Counterintuitively, this platform is growing faster than its low-code brother. El-Ouazzane said that STM32 Cube.AI’s desktop downloads grew 400% between March 2022 and May 2023.

“Here, the time to market is very fast—less than two years—because the people on this platform know what they want and know how to deploy, and the level of sophistication is pretty high,” he said.

El-Ouazzane knows that AI software is both a compiler issue and a toolchain issue. Armed with the knowledge that it would be difficult to get developers to change from familiar toolchains, ST approached Nvivd with the idea of working with its popular Tao toolchain. The resulting collaboration means models from Nvivd’s or ST’s model zoo, in ONNX format, can be ported to the Tao toolchain, trained and optimized (quantized and pruned) and then converted back to ONNX to export to STM32 Cube.AI for compilation to C code that can run on the STM32.

“Here, the mindset was: There is a reference toolchain, and the more we integrate into it, the more we can expand the universe of developers and the downloads we’ve got,” El-Ouazzane said. “I believe Nvivd sees there is a huge market of 500 million microcontrollers per year, and [the models] have to be trained somewhere.”

ST’s example application shows an STM32 MCU executing person detection before handing off only images with people in them to an Nvivd Jetson GPU for further classification tasks. This reduces the
with an official launch next year. However, El-Ouazzane is clear that the N6 is not the end goal for ST in AI.

“If we nominally say we want to reach our performance-per-watt end goal between 2025 and 2030, you can assume N6 is one-tenth of the way there,” he said. “That’s the amount of boost you’re going to see in the coming years. The N6 is a kick-ass product, and it is getting a lot of traction in AV-centric use cases, but there is an explosion of performance coming: There will be neural networks on microcontroller fusing vision, audio and time-series data.”

His vision for the required 10× performance jump is that nonvolatile memory, which enables analog compute-in-memory schemes, is critical.

ST presented a paper at ISSCC this year about an SRAM-based in-memory compute design it is developing for future generations. The demonstrator achieved 57 TOPS at 77 TOPS/W at the chip level (at INT4). However, it may be a little while before this reaches the mass market.

“The technology is in silicon today—we can demonstrate it and measure its performance,” El-Ouazzane said. “But it is becoming a question of roadmap intersect. This is something that will come in the next three to five years, for sure.”

For ST, he points out, when it comes, it will come at scale.

Getting a product ready for that kind of volume takes time—testing, documentation, support—so the timing has less to do with technology and more to do with how quickly ST can turn technologies into mass-market products.

“ST has made a number of boards available in its dev cloud for each STM32 part.
(Source: STMicroelectronics)
ADVERTORIAL

Precious Mountain: World’s First Professional Cleanroom Biomass Gloves

The demand for professional cleanroom disposable gloves has emerged as a key driving force in the global cleanroom supplies market. In 2022, the market for cleanroom equipment reached a significant value of US$3.9 billion, with the biopharmaceutical industry serving as the largest end user of cleanrooms, closely followed by the electronics industry. The introduction of various certifications, including national safety and quality health standards as well as ISO inspections, has further contributed to the heightened demand for cleanrooms in the biopharmaceutical and electronics sectors. The latter stages of the Covid-19 pandemic have emphasized the criticality of infection-control measures, resulting in an increased need for cleanroom consumables in areas associated with pharmaceuticals, vaccines and medical device research and manufacturing. Moreover, in December 2020, 19 member countries of the European Union signed the Semiconductor and Processor Technology Initiative with the aim of revitalizing the EU’s global position in the semiconductor field. This development indicates significant growth opportunities in the market for cleanroom consumables.

INNOVATION & BREAKTHROUGH: A GLOBAL FIRST—PROFESSIONAL CLEANROOM BIOMASS GLOVES

Precious Mountain, widely recognized as PM Group, has introduced a pioneering advancement in the glove industry. Demonstrating its steadfast commitment to environmental sustainability, PM Group has successfully developed the world’s first vinyl biomass glove: Bio-Mass. This revolutionary patented technology has also been seamlessly integrated into the production process of professional cleanroom gloves, marking a significant milestone in the development of the groundbreaking PVC PACER Bio-Mass Gloves.


The PVC PACER Bio-Mass Gloves have received three prestigious global certifications: JORA from Japan, USDA from the United States and OK Biobased from Europe.

- The patented technology behind the PVC PACER Bio-Mass Gloves involves the substitution of a portion of petrochemical raw materials in traditional vinyl gloves with biomass materials. Biomass, derived from living or recently deceased organisms, serves as a sustainable alternative. Through a series of processing and consumption cycles, along with the utilization of carbon dioxide generated during plant photosynthesis, the PVC PACER Bio-Mass Gloves achieve an outstanding carbon-neutral characteristic.

- PVC PACER Bio-Mass Gloves represent a revolutionary and environmentally friendly innovation within the disposable glove industry, embodying the company’s unwavering commitment to environmental protection, social responsibility and sustainable business practices.

ABOUT PM GROUP

Founded in 1978 in Taipei, Taiwan, PM Group has established itself as a distinguished medical device company. With over four decades of expertise in professional research, production and manufacturing, PM Group remains dedicated to its mission of “Quality You Can Trust.” With a focus on continuous exploration and development of professional glove products, the company has emerged as a leading force in the industry.

Beyond medical gloves, PM Group’s product range extends to cater to various sectors, including laboratories, the electronics industry, the food and beverage sector and the automotive repair industry. Committed to delivering excellence, the company’s disposable gloves consistently uphold the highest standards of quality and value.

To meet the ever-growing global demand for disposable gloves, PM Group expanded its production capabilities beyond Taiwan in 2006, venturing into China and Vietnam. The strategic integration of the supply chain across three locations and six factories empowers PM Group to effectively serve the glove needs of diverse industries worldwide, further solidifying its position as a trusted and preferred supplier.

INTRODUCTION TO THE PACER SERIES

PM Group’s PACER series of professional cleanroom gloves is specifically designed to meet the strict requirements of environments with precise control over airborne particle concentration, such as cleanrooms and laboratories. These gloves undergo a series of specialized cleaning processes, including precise material composition, precise molding and rigorous vacuum packaging, to ensure exceptional product characteristics, such as low particle shedding, low ion content and rapid static dissipation. Striving for excellence, these gloves adhere to the highest standards, meticulously excluding all potential environmental factors that could lead to product contamination, making them the ideal choice for cleanroom environments.

In industries where environmental conditions are of utmost sensitivity, such as semiconductors, green energy, solar energy, pharmaceuticals and biotechnology, cleanroom gloves from the PACER series are extensively utilized. With their unparalleled performance and reliability, these gloves provide the assurance and confidence required for critical tasks within these specialized industries.

The PACER Electronic Professional Cleanroom Gloves possess the following key features:

- Low particle content and low extractable ions: Minimize contamination of sensitive components
- Electrostatic-discharge properties: Safely
World’s First Professional Cleanroom Biomass Gloves

and quickly dissipate static electricity, reducing the risk of damaging sensitive electronic components

- (ISO 4) Class 10 cleanroom environment packaging: Ensures glove integrity and prevents contamination in high-grade cleanroom isolation environments
- Non-allergenic formula: Made from 100% non-natural latex, eliminating the risk of natural latex allergies
- Skin-friendly comfort and dexterity: Allows for extended wear while maintaining hand dexterity, enabling precise and comfortable handling, even when dealing with intricate components

SUITABLE APPLICATIONS & ENVIRONMENTS

The PACER cleanroom gloves are primarily designed for high-tech, precision -controlled cleanroom environments, catering to industries like technology, semiconductor and aerospace and defense. In these industries, the presence of particles, dust or dirt can severely impact the accuracy of microelectronic products. PACER cleanroom gloves serve as a critical component in upholding the quality and performance of microelectronic products, ensuring they meet the required specifications. Moreover, PACER cleanroom gloves find suitability in various applications within the green energy and solar energy industries, including fuel cells, batteries and energy storage systems.

Amid the impact of the Covid-19 pandemic, the pharmaceutical and biotechnology industries have experienced significant growth. To prevent contamination and minimize the dispersion of dust and particles during the manufacturing process of medications, biopharmaceuticals, vaccines, medical devices and other products, the use of PACER cleanroom gloves designed for prolonged wear can enhance precision and operational sensitivity in research and production.

AVAILABLE PRODUCTS

With over 40 years of experience, Precious Mountain stands as a prominent global professional glove manufacturer, specializing in the development, production and manufacturing of high-standard medical gloves. With the same rigorous approach, the company has extended its product range to the field of cleanroom gloves.

The PACER Professional Cleanroom Gloves are available in two materials: vinyl (synthetic polymer) and nitrile (acrylonitrile butadiene synthetic rubber). The choice of material can be made based on industry application and operational requirements:

- Vinyl: Effectively blocks contaminants and chemical erosion and is latex-free, eliminating concerns for latex allergies
- Nitrile: Provides superior elasticity, flexibility, durability, chemical resistance and puncture resistance and is a preferred choice for medical and laboratory applications

To meet the diverse needs of customers, PACER offers two options: standard-length (230 mm) and extended-length (290 mm) gloves. The extended-length gloves provide additional coverage and protection for the wrists and forearms, effectively isolating contact with the cleanroom environment.

Manufactured in compliance with ISO 9001 and ISO 13486 quality management systems, the gloves ensure consistency in quality and performance. A wide range of cleanroom gloves, from ISO 4 to ISO 6 and above, is available to meet different requirements. Customization of various sizes and specifications are offered to tailor to unique customer needs.

Advantages

The PACER cleanroom gloves from PM Group offer numerous advantages:

- Excellent tensile strength
- High durability, reducing the risk of tearing or puncturing during use
- Outstanding elongation rate, surpassing ASTM standards
- Excellent stretchability and elasticity, providing a comfortable fit and minimizing fatigue during prolonged wear
- Stringent cleanliness standards, vacuum-sealed packaging to ensure complete vacuum and protection during transportation and storage
- Customizable high-grade anti-static vacuum bags based on customer requirements

The exceptional performance and high-quality standards of PACER Professional Cleanroom Gloves have gained recognition from international semiconductor wafer fabs and panel manufacturers. Notably, companies like Innolux Corporation, United Microelectronics Corporation (UMC) and Samsung Electronics, among others, have designated PACER as their preferred choice for cleanroom gloves.

STREAMLINED SHIPMENT, TIMELY DELIVERY ENHANCE CUSTOMER SATISFACTION

PM Group has established its production bases in three key locations across Asia: Taiwan, Vietnam and mainland China, with a total of six state-of-the-art factories operating in these regions, enabling the company to efficiently meet the demands of its global clientele. Its highly skilled sales and service team takes great pride in providing optimized and tailored product offerings and technical services, ensuring that optimal solutions align with the unique requirements of customers. Regardless of proximity, PM Group offers convenient shipping options that encompass efficient sea transportation, allowing the company to handle heavy shipments with ease and guaranteeing timely and reliable delivery to clientele around the world.

PROACTIVE SOLUTIONS, INNOVATIVE SERVICES

PM Group takes immense pride in cultivating enduring partnerships with customers from more than 100 countries across all five continents. Beyond meeting their needs, it actively engages in providing proactive and tailored product solutions that perfectly align with their diverse requirements. Driven by a commitment to customer satisfaction, PM Group consistently pursues innovation across its products and services. Through collaborative teamwork serving as the backbone of operations, the company strives to fulfill the comprehensive purchasing needs of diverse industries and aims to exceed customer expectations.

PM Group specializes in the professional research and production of various disposable gloves and welcomes all inquiries and offers comprehensive integration services for all disposable glove needs. Please visit www.pmgloves.com for more information.

www.eetimes.eu | SEPTEMBER 2023
The U.K. government released its National Semiconductor Strategy in May. The document sets out the U.K. government’s vision for the semiconductor industry in the U.K., detailing its plans for funding and other initiatives to support the sector. The strategy also details how the U.K. can be more resilient to supply chain shocks and how it can deal with the threats to national security that arise from semiconductor technology.

The U.K. government has promised up to £200 million (about €231 million) for the sector over the next three years, with the possibility of £1 billion (about €1.15 billion) over the next 10 years. Those numbers are relatively small compared with the tens of billions on offer elsewhere and therefore have predictably drawn considerable attention and criticism. Such comparisons are not particularly helpful, however. As we’ll see below, the U.K.’s objectives are somewhat different from those of other countries. For a start, it is not trying to onshore the entire semiconductor supply chain.

**THE U.K. GOVERNMENT’S VISION**

The strategy’s overarching vision focuses on the U.K.’s main strengths: R&D, design and intellectual property, and compound semiconductors. There are no surprises here. The U.K. already has an excellent university-based research base with a strong record in spinning out successful semiconductor companies. Design and IP refers to design companies like Arm and Imagination—two huge success stories—and the many smaller companies that follow in their steps. And the compound semiconductor cluster in South Wales is well known to have world-leading R&D in that field.

On the other hand, the strategy does not address manufacturing, acknowledging that the U.K. is not going to compete with Taiwan, China, the U.S. or even Europe when it comes to silicon-based semiconductor production.

**GROWING THE U.K. SECTOR**

The strategy pays particular attention to R&D, focusing on university spinouts and startups. It acknowledges that while funding is already available through various funding bodies, semiconductor companies must compete with other technologies. A more focused approach is needed. It therefore identifies innovative manufacturing technologies and several emerging semiconductor technologies as target areas for available funding. The focus is on university-based R&D and spinouts. There are also proposals for funding doctoral research in key semiconductor technologies.

One of the most interesting parts of the strategy for many companies is the proposed launch of a U.K. Semiconductor Infrastructure Initiative, which would research the infrastructure required to enable more commercial R&D in the U.K. The initiative includes the possibility of an “open foundry” for compound semiconductors, as well as access to chip design software and prototyping facilities. Such services are typically highly expensive to access and are often based outside of the U.K., creating problems for small and medium enterprises (SMEs) with limited resources. The initiative is currently in a consultation phase, with an initial report expected in the fall.

Another interesting proposal is for the establishment of a semiconductor incubator. The aim here is to lower the barriers to entry for startups by providing business coaching as well as access to design tools and prototyping.

Beyond this, much of the “growing the U.K. sector” strand is about nurturing skills and talent. Many initiatives are mentioned, from incentives for teachers in the sciences to support for STEM outreach programs for semiconductors. While growing the talent pool is a hugely important and valuable part of the strategy, it will be some time before semiconductor companies feel the benefits.

The strategy also mentions various aspects that were already announced as part of the spring budget. For example, a higher rate of tax relief will be available for R&D-intensive SMEs. A program designed to encourage pension companies to invest in science and technology and the government’s new investment zones were also highlighted as areas that would benefit the semiconductor sector.

**SAFEGUARDING U.K. SUPPLY CHAINS**

Like other countries, the U.K. government has acknowledged that semiconductor supply chain disruptions can have a negative impact on industry and national security. The strategy includes several provisions to address this problem. For example, the government will publish guidance to help companies prepare for future shocks to supply chains. The strategy also proposes various
information-gathering exercises to look at the impact of future shortages on critical sectors and to ensure resilient supply to the defense sector.

The government will review the manufacturing requirements of critical sectors in the U.K. to establish the baseline level of manufacturing that would be required to ensure the U.K. remains resilient. The strategy also proposes several initiatives that will involve international collaboration with trusted partners to improve supply chain resilience.

The strategy focuses on the U.K.’s main strengths: R&D, design and IP, and compound semiconductors.

Much of this resembles similar initiatives under the EU Chips Act. For example, the EU legislation includes provisions relating to European R&D and supply chain monitoring. It will be interesting to see what steps are taken to work with the EU on information-sharing schemes to maximize the benefit of these initiatives.

PROTECTING THE U.K. AGAINST SECURITY RISKS

The strategy identifies two areas that are relevant to national security: the risk of U.K. technology getting into the wrong hands and being used against U.K. interests, and the threat posed by cybersecurity vulnerabilities built into semiconductor hardware.

The government has already used the National Security and Investment Act to block the sale of U.K.-based semiconductor companies to Chinese-backed entities. This was the case with the sale of the Newport Wafer Fab to Nexperia. The strategy acknowledges that the way the government has used this legislation has come in for criticism, however, and advises a more transparent approach. For example, it proposes that the government provide guidance on which parts of the sector it regards as more sensitive. The strategy also proposes the potential expansion of export controls to certain semiconductor technologies.

As for cybersecurity, the strategy acknowledges that the U.K. has a leading part to play in ensuring that hardware-based security is up to the job, given the country’s strength in hardware design and IP. The strategy proposes various initiatives to continue the U.K.’s role in this field, including convening experts from across the sector to discuss security improvements and facilitating discussions with our international partners on the issue of security.

The strategy also focuses on the RISC-V instruction set, acknowledging the U.K.’s strong position in this technology. It proposes government support for academic research and collaboration with industry to further the U.K.’s capabilities.

WHAT DOES THIS MEAN FOR U.K. BUSINESSES?

The strategy’s vision and focus on semiconductors should be broadly welcomed by the U.K. semiconductor sector. However, there are definite winners and losers here. Universities, spinouts and startups stand to gain more than some of the U.K.’s more established semiconductor companies.

The compound semiconductor cluster in South Wales and the companies participating in the design and IP links of the supply chain will be pleased to see that the U.K.’s strengths in these areas are recognized. University spinouts and startups will be pleased to see promises of government funding for certain types of manufacturing capability and emerging technologies. The provision of extra support for academic training and tax relief for R&D-intensive startups will also be welcomed.

There is, however, a significant group of companies that may suspect there’s not much for them in the strategy’s proposals. These are the established larger companies, some of which have manufacturing capacity in the U.K. They might have been hoping for more support in terms of R&D tax relief, public sector procurement, export support and other financing and investment initiatives. While it might be argued that these companies don’t require government support, the U.K. doesn’t operate in a bubble. This part of the U.K. sector will certainly be considering carefully how initiatives in the U.S. and EU compare with what is available here.

Additionally, we will have to wait to find out more about certain aspects of the strategy. For example, the first report on the U.K. Semiconductor Infrastructure is not due until the fall. Furthermore, the U.K. Semiconductor Advisory Panel was meant to be announced in June, and we are still waiting for the panel’s composition to be announced. While it takes time to get new initiatives moving, some may regard these delays as frustrating, given the pace at which other countries and regions are moving on semiconductor policy.

At this stage, it is clearly too early to say what impact the strategy will have on the U.K. sector. The early signs are positive, but how the money is deployed and how effectively the different elements of the strategy are implemented will be key to its success.

Andrew Thompson is partner and U.K. and European patent attorney at patent law firm EIP.

Assessing the U.K. National Semiconductor Strategy

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The FCC and NCAP have drafted regulations requiring OEMs to install a child presence detection (CPD) system in new cars. The most promising technology for in-cabin monitoring systems in general and for CPD in particular is radar, allowing the reliable detection of target objects in the car.
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Read more in the article starting on page 38.
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